

Loongson 7A1000 Bridge User Manual

Loongson Technology Corporation Limited

Version 2.00

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About this manual

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Reading Guide

This manual describes the overall bridge architecture, clock structure, address space, configuration registers, and individual functional interfaces, primarily for BIOS and kernel developers.

Translator's Note

These documents were translated by Yanteng Si and Feiyang Chen.

This is the translation of <https://github.com/loongson/LoongArch-Documentation/releases/latest/download/Loongson-7A1000-usermanual-v2.00-CN.pdf>.

Due to the limited knowledge of the translators, there are some inevitable errors and omissions existing in this document, please feel free to correct.

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Since the release of the project, we have gotten several errata and content changes donated. Here are all the people who have contributed to [LoongArch Documentation](#) as an open source project. Thank you everyone for helping make this a better book for everyone.

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Chapter 1. Introduction

1.1. Introduction to this Manual

1.1.1. Contents of the Chapters

Section 1 is an introduction that provides an overview of the features and functions of this bridge chip.

Section 2 introduces the bridge chip clock structure, describes the clock of the bridge chip, and details the clock-related hardware configuration and software usage.

Section 3 introduces the address space of the bridge chip, describing the entire address space of the processor (Loongson 3 processor) + bridge chip and the address space distribution inside the bridge chip.

Section 4 introduces the bridge chip configuration registers.

Section 5 introduces interrupts.

Section 6 describes the HPET controller.

Section 7 introduces the HT controller.

Sections 8-14 describe the low-speed interface and other internal functions of the bridge chip. These include: address space description, UART serial controller, I2C controller, PWM controller, and other internal functions. I2C controller, PWM controller, ACPI power management module, real-time clock RTC, and GPIO interface.

Section 15 describes the GMAC controller.

Section 16 describes the USB controller, including the EHCI controller and the OHCI controller.

Section 17 describes the Graphics Processing Unit GPU.

Section 18 describes the display controller DC.

Section 19 describes the HDA controller.

Section 20 describes the AC97 controller.

Section 21 describes the SATA controller.

Section 22 describes the PCIE controller.

Section 23 introduces the SPI controller.

Section 24 introduces the LPC controller.

Appendix 1 explains the chip pin multiplexing relationship.

Appendix 2 gives the software usage notes.

1.1.2. Conventions of this Manual

Note: The bit field of Reserved in the register description in the text is either a read-only attribute or a read-write attribute. Regardless of the attribute of the bit field, the software must ensure that the value of the bit field is not changed, that is, if the software needs to modify a register containing a Reserved bit field, it must ensure that the value written to the Reserved bit field is the same as the value read from the bit field.

For ease of presentation, the following abbreviations are used to denote the register attributes.

R0 Read-only

WO Write-only

R/W Read-Write

R/WC read-write, write clear

1.2. Overview of the Bridge

The Loongson 7A1000 bridge chip (hereafter referred to as the bridge chip) is Loongson's first dedicated chipset product, providing north-south bridge functionality for Loongson processors. The bridge chip is connected to the Loongson Series 3 processor via the HT high-speed bus interface and has an integrated GPU, DisplayController, DDR3 SDRAM memory controller, and PCIE, SATA, USB, GMAC, I2C, UART, GPIO, and other interfaces.

Main Characteristics of the Bridge Piece

- 16-bit HT 3.0 interface
- Support dual-way bridge chip mode
- 2D/3D GPU
- Display controller, supports dual DVO display
- 16-bit DDR3 graphics memory controller
- 3 x8 PCIE 2.0 interfaces, each x8 interface can be split into 2 independent x4 interfaces
- 2 x4 PCIE 2.0 interfaces that can be split into 6 independent x1 interfaces
- 3 SATA 2.0 ports
- 6 USB 2.0 ports
- 2 RGMII Gigabit LAN interfaces
- HDA/AC97 configurable interface
- RTC support
- HPET support
- UART interface
- I2C interface
- LPC interface
- SPI interface
- GPIO interface
- Support ACPI specification
- Support JTAG bound scan

1.3. Main Functions of the Bridge

HT Interface

The bridge is connected to the processor via the HT interface, which is compatible with HT3.0 protocol and supports 200/400/800/1600Mhz interface frequency and 8/16-bit interface width. In addition to being used as a single bridge chip, it can also be configured as a dual bridge chip mode to support direct data transfer with both processors.

Graphics Processing

The GPU supports OpenGL ES 2.0 and OpenGL ES 1.1; OpenVG, Futuremark certified, BitBLT and Stretch BLT, rectangle fill, hardware line drawing, color font rendering, YUV color space conversion, and high quality scaling. Space conversion, high quality scaling, etc. The display controller supports dual DVO signal output and hardware cursor, gamma correction, output dithering, etc. The memory interface uses 16-bit DDR3 SDRAM interface with a maximum data rate of 1333 Mbps.

PCIE Interface

The PCIE 2.0 protocol-compliant interface contains a total of 32 data links supporting up to 5G b/s in each data direction (10G b/s in both directions) and a total of 12 PCIE controllers. 32 data links can be divided into 3 x8 interfaces and 2 x4 interfaces; each x8 interface can be configured as 2 x4 interfaces. Each x8 interface can be configured as two x4 interfaces independently; of the two x4 interfaces, one can be configured as four x1 interfaces independently, and the other as two x1 interfaces independently.

SATA Controllers

Integrated 3 SATA host controllers, each controlling 1 SATA interface, each supporting up to 3 Gb/s data rate and compatible with SATA 2.6 protocol. SATA controllers are compatible with AHCI 1.1 specification.

USB Controllers

Two USB controllers control six independent USB host interfaces, supporting up to USB 2.0 protocol with maximum transfer speeds of up to The two USB controllers control six independent USB host interfaces, supporting up to USB 2.0 protocol and transfer speeds up to 480 Mbps, and are compatible with USB 1.1 full-speed and low-speed transfers.

GMAC Controller

Integrated two 10/100/1000Mbps adaptive Ethernet MAC controllers, compatible with IEEE 802.3, connect external GMAC PHY chip through RGMII interface, half-duplex/full-duplex adaptive, support Timestamp function, support network wake-up.

HDA Controller

Supports 16, 18 and 20-bit sampling accuracy, variable rate, sampling rate up to 192KHz, 7.1 channel surround sound output, and three audio inputs.

SPI Controller

Integrated SPI host controller, supports standard read, sequential address read, fast read, dual I/O and other read modes.

UART

Integrated 1 full-featured UART controller, full-duplex asynchronous data receive/transmit, 16-bit programmable clock counter, support receive timeout detection, configurable as 4 two-wire serial ports (TXD/RXD).

I2C Bus

Compatible with I2C standard, operates in master device mode, supports 7-bit addressing and 10-bit addressing modes.

PWM

Four PWM outputs with internal 32-bit counter, supporting pulse generation and detection.

HPET

Compatible with HPET specification, supports 64-bit counter timestamp function, 32-bit timer, 1 periodic interrupt and Supports 1 periodic interrupt and 2 non-periodic interrupts.

RTC

Timing accurate to 0.1 second, can generate 3 timing interrupts, supports timed power-on function.

Interrupt Controller

Internal integrated interrupt controller supports up to 64 interrupt sources, dual interrupt outputs, software set interrupts, configurable trigger mode, and intelligent interrupt distribution.

ACPI Power Management

Supports clock gating, PHY shutdown, USB/GMAC wake-up, and auto-start for incoming calls.

GPIO

1 dedicated GPIO pin, 56 multiplexed GPIO pins, support input interrupt function.

1.4. Structure of the Bridge

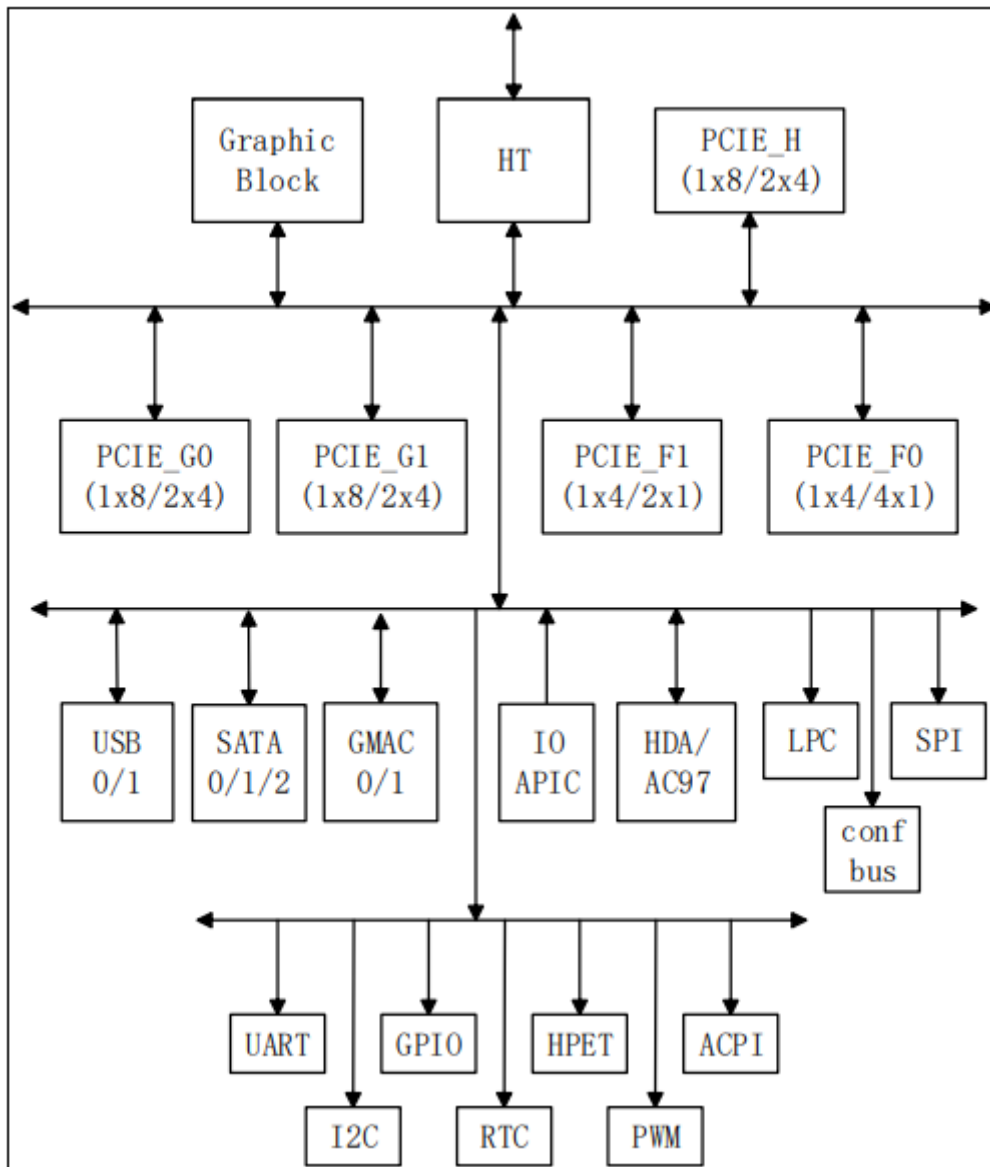


Figure 1. Structure of the Bridge

Chapter 2. Bridge and System Clock

2.1. Bridge Clock

The bridge requires a 100Mhz clock and a 32.768 K crystal as reference clock input (and a 33Mhz clock input if using the LPC bus)

Table 1. Bridge clock

| Clock | Frequency | Description |
|------------------|-----------|--|
| RTC_X0 | 32.768KHz | 32.768KHz Crystal Output |
| TESTCLK | - | Reserved |
| LPC_CLKIN | 33Mhz | LPC 33Mhz reference clock, unconnected when not using LPC interface |
| HTCLKp/n | 200Mhz | HT 200Mhz differential reference clock, unconnected |
| PCIE_F0_CLKINp/n | 100Mhz | PCIE_F0 100Mhz differential reference clock, unconnected |
| PCIE_F1_CLKINp/n | 100Mhz | PCIE_F1 100Mhz differential reference clock, unconnected |
| PCIE_H_CLKINp/n | 100Mhz | PCIE_H 100Mhz differential reference clock, unconnected |
| PCIE_G0_CLKINp/n | 100Mhz | PCIE_G0 100Mhz differential reference clock, can be left unconnected |
| PCIE_G1_CLKINp/n | 100Mhz | PCIE_G1 100Mhz differential reference clock, unconnectable |
| SATA0_CLKINp/n | 100Mhz | SATA0 100Mhz differential reference clock, do not connect |
| SATA1_CLKINp/n | 100Mhz | SATA1 100Mhz differential reference clock, do not connect |
| SATA2_CLKINp/n | 100Mhz | SATA2 100Mhz differential reference clock, do not connect |
| USB_XI | 12Mhz | Reserved |
| USB_CLKIN | 12Mhz | 12Mhz crystal input |

Note: Input clocks not provided need to be grounded through a 10Kohm resistor.

Table 2. Birge clock output

| Clock | Frequency | Description |
|------------|-----------|---|
| CLKOUT33M | 33.3MHz | 33.3Mhz single-ended clock output. Can be used as a memory reference clock for the Loongson 3 processor. |
| CLKOUT100M | 100Mhz | 100Mhz single-ended clock output. Can be used as a reference clock for the HT for the Loongson 3 processor. |

| Clock | Frequency | Description |
|-------------|-----------|--|
| CLKOUT25M1 | 25Mhz | 25Mhz single-ended clock output. Can be used as a core reference clock for the Loongson 3 processor. |
| CLKOUTFLEX1 | Variable | Variable frequency single-ended clock output. Default is 100Mhz. |

Note: 1. The CLKOUT25M and CLKOUTFLEX pins can be multiplexed as GPIO functions.

2.2. Clock-related Configuration Pins

The bridge chip sets a number of pins to set the bridge clock generation method, these configuration pins are mainly used as a backup design, the normal motherboard design does not need to change the value of these configuration pins except for CLKSEL[7:6] (dangling or kept as default values). Bridge clock-related configuration pins are shown in the following table:

Table 3. Bridge chip clock-related configuration pins and descriptions

| Pin | Direction | Default Value | Description |
|-----------------|-----------|---------------|--|
| SYS_CLKSEL[1:0] | |: | 00b | Reserved |
| SYS_CLKSEL[3:2] | |: | 00b | Reserved |
| SYS_CLKSEL[5:4] | |: | 01b | Reserved |
| SYS_CLKSEL[6] | |: | 0 | HT PHY reference clock selection. 0: Use 200MHz differential input clock. 1: Use the 100MHz system input clock. |
| SYS_CLKSEL[6] | |: | 1 | HT frequency configuration mode (recommended setting is 0). 0: The HT clock is configured in software mode. If the PLL frequency of the HT is not modified using software, the HT bus frequency remains fixed (HT1.0 mode: 200MHz; HT3.0 mode: 400MHz). 1: The HT clock can only be used in hardware configuration mode. In this case, software modification of the HT PLL frequency is not valid, and only a few frequencies can be selected via registers. For HT1.0 mode, 2: 400MHz; 5/9: 800MHz; others: 200MHz;. For HT3.0 mode, 2: 800MHz; 5/9: 1600MHz; others: 400MHz. |
| SYS_CLKSEL[6] | |: | 0 | Reserved |

2.3. Description of Clock Function

The bridge contains multiple PLLs and clock divider modules to generate the individual clocks needed for the bridge.

The bridge contains 5 PLLs, each of which can provide up to 3 clock outputs. The five PLLs are used for the following purposes

- A device PLL to generate the clocks for USB/SATA, GMAC.
- A graphics PLL to generate clocks for GPU, DC, and graphics memory.
- One system PLL to generate clocks for the internal bus, HDA bitclk, flex clkout.
- Two PIX PLLs for generating two independent pixel clocks to support dual independent displays.

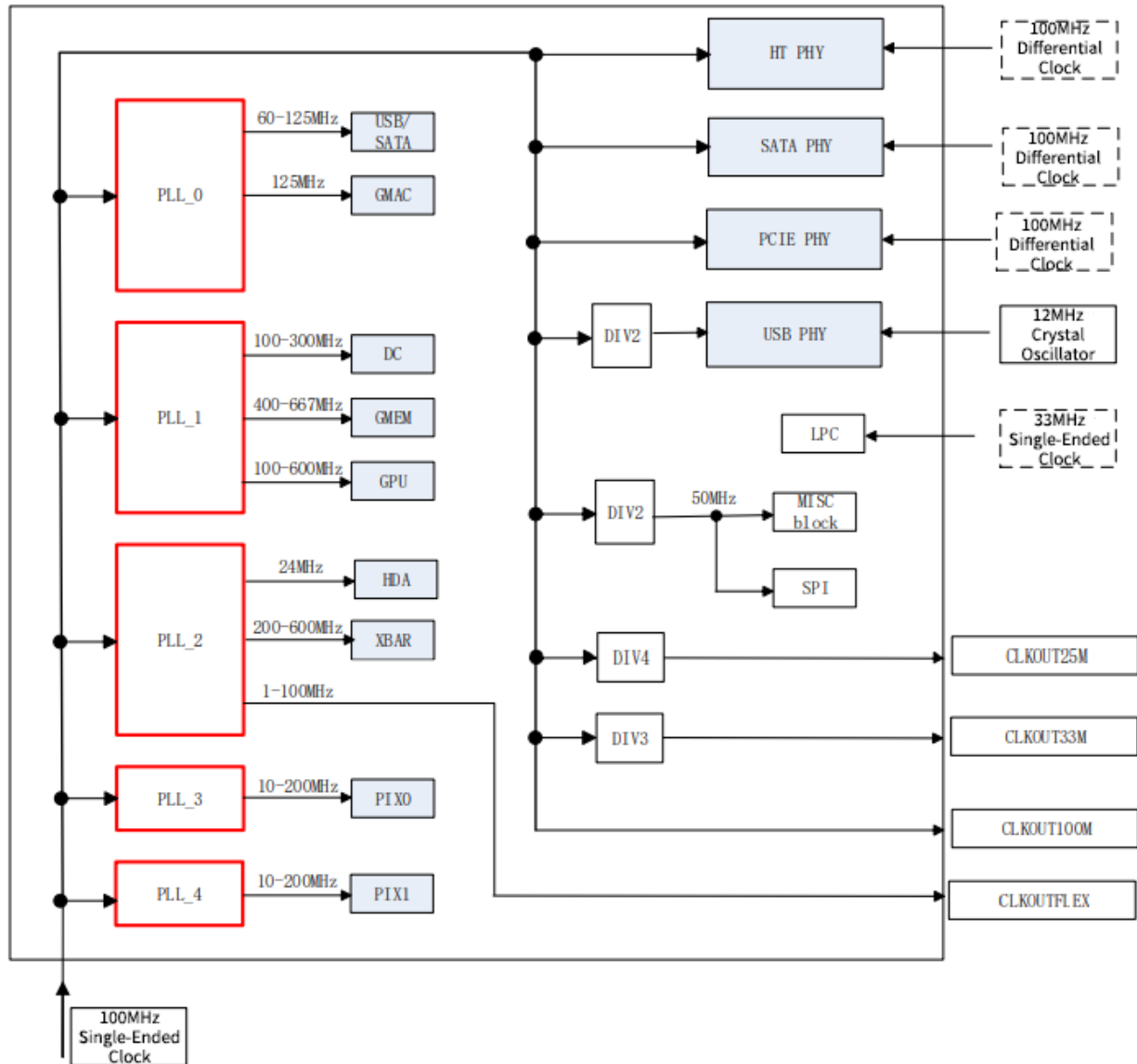


Figure 2. Structure of bridge clock

2.4. Description of PLL Function

The output clock frequency is calculated as follows.

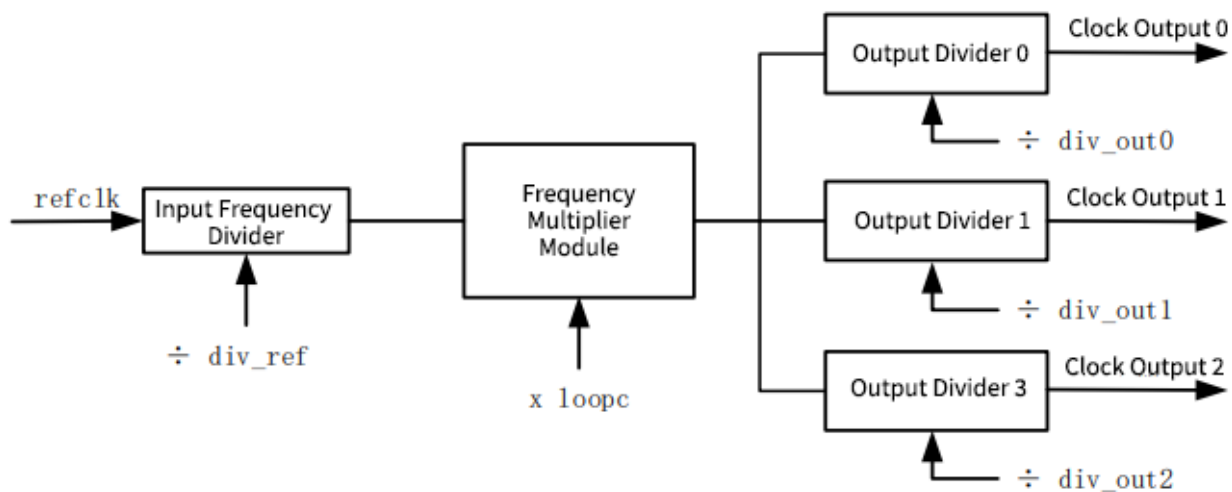


Figure 3. Structure of PLL

$$\text{clock_out} = \text{refclk} / \text{div_ref} * \text{loopc} / \text{divoutN}$$

The refclk of 7A is fixed at 100MHz, and the output of the input divider ($\text{refclk} / \text{div_ref}$) needs to be guaranteed to be in the range of 20 In addition, it is necessary to ensure that the output of the input divider ($\text{refclk} / \text{div_ref}$) is in the range of 20 - 40MHz, and the frequency after frequency doubling module ($\text{refclk} / \text{div_ref} * \text{loopc}$) is in the range of 1.2GHz - 3.2GHz.

The PLL-related configuration signals and their descriptions are shown in the follow table. The locations of these configuration signals are shown in Section 4 Bridge Configuration Registers.

Table 4. PLL-related configuration signal description table

| Signal | Digit | Direction | Description |
|---------------|-------|-----------|----------------------------------|
| pll_div_out0 | 7 | R/W | PLL output clock 0 divisions |
| pll_div_out1 | 7 | R/W | PLL output clock 1 divisions |
| pll_div_out2 | 7 | R/W | PLL Output Clock 2 Divisions |
| pll_loopc | 9 | R/W | PLL Multiplier |
| pll_div_ref | 7 | R/W | PLL Input Divider |
| pll_locked | 1 | RO | PLL Lock |
| sel_pll_out0 | 1 | R/W | Select PLL Output Clock 0 |
| sel_pll_out1 | 1 | R/W | Select PLL Output Clock 1 |
| sel_pll_out2 | 1 | R/W | Select PLL Output Clock 2 |
| set_pll_param | 1 | R/W | Set PLL configuration parameters |
| pll_bypass | 1 | R/W | PLL internal bypass |
| pll_pd | 1 | R/W | PLL powerdown |

2.5. Configuration Method of PLL

When `SYS_CLKSEL[1:0]` is `00b`, it means the output frequency of PLL can be changed by software. In this configuration, the default clock frequency at bridge startup is the external reference clock frequency,

and software configuration of the bridge clock is required during processor startup. The process of modifying the clock configuration through software is as follows:

1. set `sel_pll_out*` to 0.
2. set the `pll_pd` signal to 1.
3. set `set_pll_param` to 0.
4. set the value of `pll_div_ref/pll_loopc/pll_div_out*`.
5. set `set_pll_param` to 1.
6. set the `pll_pd` signal to 0.
7. wait for the PLL lock signal `pll_locked` to change to 1.
8. set `sel_pll_out*` to 1.

Chapter 3. Address Space

3.1. Overview of Loongson 3 and Loongson 7A Address Space

As a bridge for the HT interface, the bridge supports a 40-bit address space internally. Without the SWIOTLB, the Loongson3 processor + bridge supports a maximum of 1TB of memory address space. To support multi-processor systems, we use a few bits (up to 4 bits) of the bridge chip's internal address as the destination node number for the bridge chip's internal device DMA access. This means that the bridge chip can support a processor system with up to 16 nodes. Considering that in practice Loongson uses systems with up to 4 nodes. Therefore, this section describes the maximum number of nodes supported. For a 4-node system, the address space size for a single processor node is 256GB.

From the CPU's perspective - that is, the device address space accessible to the CPU - the address space of a bridge chip consists of three parts: configuration space, PCI I/O space, and PCI MEM space. The address space of a bridge chip has the same form as the address space defined by PCI.

1. Configuration space: this address space is used to access the configuration headers of the devices inside the bridge chip (including devices extended through the PCIE bus), and its address composition conforms to the address organization form of PCI configuration access.
2. I/O space: This address space is used to access the I/O address space defined by the PCI protocol. Only PCIE has this address space in the bridge chip for accessing downstream devices of the PCIE controller through I/O type requests.
3. MEM space: All address spaces other than the above two address spaces are MEM spaces.

The bridge chip's configuration space corresponds to the HT bus configuration space of the HT bus, with a size of 32MB. the bridge chip's PCI I/O space corresponds to the HT bus I/O space, with a size of 32MB. the bridge chip's PCI MEM space corresponds to the HT bus MEM space, with a size of 1012GB. the PCI MEM space is used to The PCI MEM space is used to access the MEM space of the bridge's internal PCIE devices, the MEM and IO space of devices other than PCIE devices, and the bridge's configuration register space.

The latter two address spaces (PCI I/O space and PCI MEM space) are part of the overall processor address space. and the system software can assign them to any location from 0 - 1TB*. When the software accesses them, it needs to map them into HT1's address space segment via the processor's level 1 XBAR or directly add HT1's address space offset to that access address.

Note*: Except for the address segment **0x0f000000-0xfffffff**. This address segment cannot be used as a bridge device address space.

From the perspective of DMA accesses - that is, accesses to the address space initiated by the bridge chip's internal devices - the address space available includes the processor's memory space and the bridge chip's memory space. The size of the processor's memory space varies depending on the number of nodes in the system, and the total DMA address space is 1 TB. For a 4-node system, the DMA address space must be located within the lower 256 GB of the node address space so that the bridge can directly access the memory of up to 4 nodes. Devices within the bridge chip that can initiate DMA operations include: GPU, DC, PCIE, USB, SATA, GMAC, HDA, and AC97.

Both types of addresses (the bridge's address space and the processor's address space) are addressed in a uniform manner, i.e., the processor's memory space, the processor's configuration space, the bridge's configuration access space, the I/O space, and the MEM space, are all located in the same address space and do not overlap with each other. For a single node system, this address space has a maximum size of 1TB.

The access addresses of the devices inside the bridge chip (PCI I/O space and PCI MEM space) are designed to be software configurable to support device discovery and management for the PCI architecture. Each device (device block) inside the bridge contains a PCI configuration header. The

software accesses the configuration header to obtain information about the type of the device, the size of the address space supported, etc., and sets the address space of the device by configuring the device's BAR register. This approach is consistent with the 780E.

The following is an example of a Loongson 3A+ bridge chip system to illustrate the address space allocation for the entire computer system. one way of dividing the address space for the 3A+ bridge chip is shown in the following figure.

| | |
|--------------------------------------|-------------------------------|
| 7A MEM High Address Space | MEM_UP_LIMIT - 0xfc,ffff,ffff |
| Memory High Address Space | 0x8000,0000 - MEM_UP_LIMIT |
| 7A MEM Low Address Space | 0x4000,0000 - 0x7fff,ffff |
| Processor Configuration Space | 0x3000,0000 - 0x3fff,ffff |
| Reserved | 0x2000,0000 - 0x2fff,ffff |
| Processor Low-speed Device Space | 0x1f00,0000 - 0x1fff,ffff |
| Processor LPC MEM Space | 0x1c00,0000 - 0x1dff,ffff |
| 7A I/O Space and Configuration Space | 0x1800,0000 - 0x1bff,ffff |
| 7A Device Fixed Address Space | 0x1000,0000 - 0x17ff,ffff |
| Memory Low Address Space | 0x0000,0000 - 0x0fff,ffff |

Figure 4. Example of address space division for Loongson 3 processor + Loongson 7A bridge

Note: The address in the figure is the low address, not including the node number and high address.

In the address space allocation method in the figure above, the

0x0000,0000 - 0x0fff,ffff is the low 256MB memory space of the system.

0x1000,0000 - 0x17ff,fff is the fixed device address space of the bridge, which includes interrupt controller, HPET, confbus, MISC low-speed devices, and LPC. ,ffff (HT1's MEM space)

0x1800,0000 - 0x19ff,ffff is the PCI I/O space of the bridge chip, the software can allocate the I/O space of the PCIE devices in the bridge chip to this address space, which is mapped to 0xefd,fc00,0000 - 0xefd,fdff through the configuration window of the first-level XBAR, ffff (I/O space of HT1).

0x1a00,0000 - 0x1bff,ffff is the configuration space of the bridge chip, which is used to access the configuration header of the internal device of the bridge chip, and the access method is compatible with the PCI protocol, the bit[23:8] of the address bit corresponds to the bus number, device number and func number in order, and this address is mapped to 0xefd, fe00,0000 - 0xefd,fff,fff (HT1's bus configuration space).

0x1c00,0000 - 0x1dff,ffff is the LPC MEM address space of 3A.

0x1f00,0000 - 0x1fff,ffff is the 3A's LPC device space.

0x2000,0000 - 0x2fff,ffff is the reserved space for the processor.

0x3000,0000 - 0x3fff,ffff is the configuration space for 3A.

0x4000,0000 - 0x7fff,ffff is the PCI MEM space of the bridge chip. This address is mapped to 0xe00,4000,0000 - 0xe00,7fff,fff (the MEM space of HT1) through the configuration window of level 1 XBAR.

0x8000,0000 - MEM_UP_LIMIT is the high memory address space of 3A.

MEM_UP_LIMIT - 0xfc,ffff,ffff is the PCI MEM space of the bridge. This address is mapped to 0xe00,0000,0000+MEM_UP_LIMIT - 0xefc,ffff,ffff (the MEM space of HT1) through the configuration window of Level 1 XBAR.

3.2. PCI Devices and Functions

Devices with DMA capability inside the bridge and some other devices contain a standard PCI configuration header. The devices that contain PCI configuration headers include: GPU, DC, PCIE, USB, SATA, GMAC, HDA/AC97, LPC, and SPI. the bus number, device number, and function number of each device are listed in the following table

Table 5. Configuration header access correspondence for each device

| Bus: Device: Function | Function Description |
|----------------------------|----------------------|
| Bus 0:Device 0:Function 0 | HT lo |
| Bus 0:Device 1:Function 0 | HT hi |
| Bus 0:Device 3:Function 0 | GMAC0 |
| Bus 0:Device 3:Function 1 | GMAC1 |
| | |
| Bus 0:Device 4:Function 0 | USB0 OHCI |
| Bus 0:Device 4:Function 1 | USB0 EHCI |
| Bus 0:Device 5:Function 0 | USB1 OHCI |
| Bus 0:Device 5:Function 1 | USB1 EHCI |
| Bus 0:Device 6:Function 0 | GPU |
| Bus 0:Device 6:Function 1 | DC |
| Bus 0:Device 7:Function 0 | HDA1 |
| Bus 0:Device 7:Function 1 | AC971 |
| Bus 0:Device 8:Function 0 | SATA0 |
| Bus 0:Device 8:Function 1 | SATA1 |
| Bus 0:Device 8:Function 2 | SATA2 |
| Bus 0:Device 9:Function 0 | PCIE_F0 Port02 |
| Bus 0:Device 10:Function 0 | PCIE_F0 Port12 |
| Bus 0:Device 11:Function 0 | PCIE_F0 Port22 |
| Bus 0:Device 12:Function 0 | PCIE_F0 Port32 |

| Bus: Device: Function | Function Description |
|----------------------------|----------------------|
| Bus 0:Device 13:Function 0 | PCIE_F1 Port03 |
| Bus 0:Device 14:Function 0 | PCIE_F1 Port13 |
| Bus 0:Device 15:Function 0 | PCIE_G0 port04 |
| Bus 0:Device 16:Function 0 | PCIE_G0 port14 |
| Bus 0:Device 17:Function 0 | PCIE_G1 port05 |
| Bus 0:Device 18:Function 0 | PCIE_G1 port15 |
| Bus 0:Device 19:Function 0 | PCIE_H port06 |
| Bus 0:Device 20:Function 0 | PCIE_H port16 |
| Bus 0:Device 22:Function 0 | SPI |
| Bus 0:Device 23:Function 0 | LPC7 |

Notes.

1. when hda_sel is 1, HDA controller can be discovered; when hda_sel is 0, AC97 controller can be discovered.
2. When PCIE_F0 works in x4 mode, only Port 0 is visible, Port 1-3 is not visible; when PCIE_F0 works in non-x4 mode, Port 0-3 is visible. When PCIE_F0 works in non-x4 mode, Port 0-3 is visible. 3.
3. When PCIE_F1 is operating in x4 mode, only Port 0 is visible and Port 1 is not visible; when PCIE_F1 is operating in non-x4 mode, Port 0-1 is visible. When PCIE_F1 is operating in non-x4 mode, Port 0-1 is visible. 4.
4. When PCIE_G0 is operating in x8 mode, only Port 0 is visible and Port 1 is not visible; when PCIE_G0 is operating in x4 mode, Port 0-1 is visible. mode, Port 0-1 is visible. 5.
5. When PCIE_G1 is operating in x8 mode, only Port 0 is visible and Port 1 is not visible; when PCIE_G1 is operating in x4 mode, Port 0-1 is visible. When PCIE_G1 is operating in x4 mode, Port 0-1 is visible. 6.
6. When PCIE_H is operating in x8 mode, only Port 0 is visible and Port 1 is not visible; when PCIE_H is operating in x4 mode, Port 0-1 is visible.
7. LPC(D23:F0) is only visible when LPC module is enabled.

When the bus number, device number, function number and address offset accessed by the configuration header are invalid, the write operation is invalid; the data obtained by the read operation is 0xFFFFFFFF.

3.3. Access Address of the PCI Configuration

The processor can access the configuration space of the bridge chip through two address spaces. One is the standard configuration access space defined by HT (0xFD_FE00_0000 - 0xFD_FFFF_FFFF) and the other is the reserved address space of HT (0xFE_0000_0000 - 0xFE_1FFF_FFFF). The configuration space size for each bridge device accessed through the HT standard configuration access space is 256 bytes; the configuration space size for each bridge device accessed through the reserved address space is 4K bytes.

The maximum configuration space size per device is 256 bytes when using the HT-defined standard configuration access space (0xFD_FE00_0000-0xFD_FFFF_FFFF) to access the bridge slice. The address [39:24] determines the configuration header type (0xFDFE is Type0, 0xFDFE is Type1); [23:16] indicates the Bus Number; [15:11] indicates the Device Number; [10:8] indicates the Function Number; [7:0] indicates the offset. The following diagram shows the meaning of the address segment for the CPU to access the PCI configuration space using the HT standard configuration access space

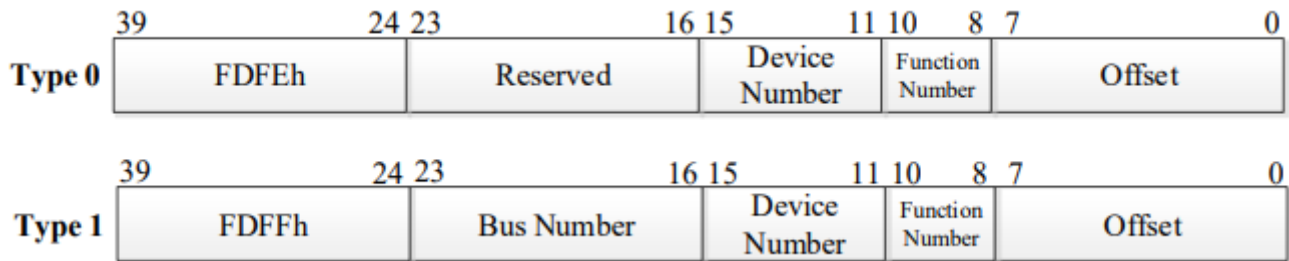


Figure 5. Standard access address of the PCI configuration

When using the HT's reserved address space (0xFE_0000_0000 - 0xFE_1FFF_FFFF) to access bridge slices, the maximum configuration space size per device is 4K bytes. The address [39:28] determines the configuration header type (0xFE0 is Type0, 0xFE1 is Type1); [23:16] indicates the Bus Number; [15:11] indicates the Device Number; [10:8] indicates the Function Number; [27:24] and [7:0] are combined to represent the offset. The following diagram illustrates the meaning of the address segment for the CPU to access the PCI configuration space using the HT reserved address space.

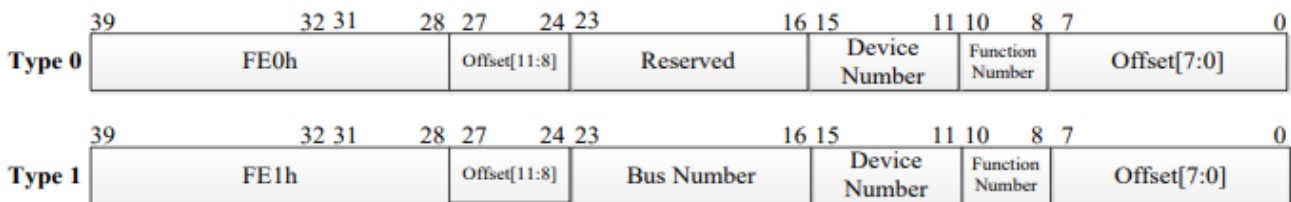


Figure 6. reserved access address of the PCI configuration

In general, it is recommended to use the HT standard configuration access space (0xFD_FE00_0000-0xFD_FFFF_FFFF) for PCI configuration header access.

3.4. Example of Bridge Device Address Space Allocation

Access to the bridge chip devices is mainly done through the PCI MEM space. The software can assign any access address for each device on the bridge chip within this address segment. The internal PCI devices of the bridge chip include: GPU/DC, GMEM, PCIE, USB, SATA, GMAC, HDA/AC97, LPC, SPI, all of which can be seen through lspci. The access addresses of these devices (except LPC) can be dynamically assigned by software. One way of allocation is as follows: by scanning the PCI bus and reading the configuration space of each device (PCI mode orientation) to get the size of MEM space and I/O space used by each device, the system software allocates the appropriate size of MEM space from the address 0x40000,0000-0x7fff,fff, and from 0x1800, 0000-0x19ff,ffff. The system software allocates the appropriate size of I/O space (PCIE devices) from 0x40000,0000-0x7fff,ffff.

In addition to these PCI type devices, the bridge also contains some devices that are accessed using fixed addresses, such as: interrupt controllers, HPET controllers, confbus In addition to these PCI-type devices, the bridge also contains devices that are accessed using fixed addresses, such as: interrupt controllers, HPET controllers, confbus configuration registers, MISC low-speed device blocks, and LPCs.

The following two tables give an example of an address allocation for a bridge chip fixed address device and a PCI device, along with their address space size and supported access types. For the access types, B indicates byte access (1byte), H indicates half-word access (2byte), W indicates word access (4byte), D indicates double-word access (8byte), Q indicates 4-word access (16byte), and C indicates cacheline access.

Table 6. Bridge piece fixed address device address space

| Module | Address space | Address space size | Access type |
|--------|---------------------------|--------------------|-------------|
| INT | 0x1000, 0000-0x1000, 0fff | 4K | BHW |
| HPET | 0x1000, 1000-0x1000, 1fff | 4K | BW |

| Module | Address space | Address space size | Access type |
|----------|-------------------------|--------------------|-------------|
| CONF REG | 0x1001,0000-0x1001,ffff | 64K | BHW |
| MISC | 0x1008,0000-0x100f,ffff | 512K | BW |
| LPC REG | 0x1000,2000-0x1000,2fff | 4K | W |
| LPC MEM | 0x1200,0000-0x13ff,ffff | 32M | BHWDQC |
| LPC I/O | 0x1800,0000-0x1800,ffff | 64K | B |
| LPC TPM | 0x1801,0000-0x1801,ffff | 64K | B |

Table 7. Bridge chip PCI device address space allocation example

| Module | Address space | Address space size | Access type |
|----------------|-------------------------|--------------------|-------------|
| GPU | 0x5ff4,0000-0x5ff7,ffff | 256K | W |
| DC | 0x5ff8,0000-0x5ff8,ffff | 64K | W |
| Graphic Memory | 0x4000,0000-0x4fff,ffff | 256M | BHWDQC |
| PCIE I/O | 0x1802,0000-0x19ff,ffff | 32M | BHW |
| PCIE MEM | 0x6000,0000-0x7fff,ffff | 512M | BHW |
| SPI MEM | 0x5e00,0000-0x5eff,ffff | 16M | BHWDQC |
| USB0-EHCI | 0x5fd0,0000-0x5fd0,7fff | 32K | W |
| USB0-OHCI | 0x5fd0,8000-0x5fd0,ffff | 32K | W |
| USB1-EHCI | 0x5fd1,0000-0x5fd1,7fff | 32K | W |
| USB1-OHCI | 0x5fd1,8000-0x5fd1,ffff | 32K | W |
| SATA0 | 0x5fe0,0000-0x5fe0,1fff | 8K | W |
| SATA1 | 0x5fe0,2000-0x5fe0,3fff | 8K | W |
| SATA2 | 0x5fe0,4000-0x5fe0,5fff | 8K | W |
| GMAC0 | 0x5fe1,0000-0x5fe1,7fff | 32K | W |
| GMAC1 | 0x5fe1,8000-0x5fe1,ffff | 32K | W |
| HDA | 0x5fe2,0000-0x5fe2,ffff | 64K | BHW |
| AC97 | 0x5fe3,0000-0x5fe3,ffff | 64K | W |
| SPI REG | 0x5ff1,1000-0x5ff1,1fff | 4K | B |

The size of the address space of the above devices is fixed, except for PCIE MEM and Graphic Memory, which can be changed by software.

The BIOS needs to modify the MASK value of the BAR register 2/3 of the GPU configuration header by accessing the bridge configuration register GMEM_BAR_MASK to configure the size of Graphic Memory. Graphic Memory size, and then the software will get the graphic memory size through PCI. The software then scans through the PCI to obtain the size of the graphics memory.

In the case of using a PCIE external discrete graphics card, the discrete graphics memory space that comes with the discrete graphics card is located in the PCIE MEM address space and is managed as a PCIE device.

Chapter 4. Bridge Configuration Register

The bridge chip sets up registers to configure certain features of the bridge chip that are not specific to a particular interface (PCIe, USB, etc.). These registers are arranged uniformly in the bridge's configuration register space (not the PCI configuration access space). The address space size of the bridge configuration registers is 64KB, and the starting address (internal space of the bridge) is configured by the BIOS.

The bridge chip configuration registers contain the following.

1. Bridge chip general configuration (0x0 - 0x47f).
2. PLL configuration (0x480 - 0x4cf).
3. PCIe controller and PHY configuration (0x580 - 0x617).
4. SATA controller and PHY configuration (0x740 - 0x76f).
5. Memory capacity configuration registers (0x3838 - 0x383f).
6. Bridge ID (0x3ff8 - 0x3fff).

Table 8. Bridge configuration register list

| Address Offset | Name | Read/Write | Description |
|----------------|---------------|------------|---|
| 0x0418 | HT_ROUTE | R/W | HT Routing Configuration |
| 0x0420 | FUNC_CONFIG0 | R/W | General Configuration Register 0 |
| 0x0430 | FUNC_CONFIG1 | R/W | General Configuration Register 1 |
| 0x0440 | PAD_CONFIG | R/W | PAD Multiplexing Configuration |
| 0x0480 | PLL_0 | R/W | PLL0 Configuration |
| 0x0490 | PLL_1 | R/W | PLL1 Configuration |
| 0x04a0 | PLL_2 | R/W | PLL2 Configuration |
| 0x04b0 | PLL_PIX_0 | R/W | PLL_PIX0 Configuration |
| 0x04c0 | PLL_PIX_1 | R/W | PLL_PIX1 Configuration |
| 0x04d0 | FREQSCALE | R/W | Device Frequency Division Configuration |
| 0x0580 | PCIE_F0_REG | R/W | PCIE_F0 Configuration Register |
| 0x0590 | PCIE_F0_PHY | R/W | PCIE_F0 PHY Configuration Access Register |
| 0x05a0 | PCIE_F1_REG | R/W | PCIE_F1 Configuration Register |
| 0x05b0 | PCIE_F1_PHY | R/W | PCIE_F1 PHY Configuration Access Register |
| 0x05c0 | PCIE_H_REG | R/W | PCIE_H Configuration Register |
| 0x05d0 | PCIE_H_PHY_LO | R/W | PCIE_H PHY Lo Configuration Access Register |
| 0x05d8 | PCIE_H_PHY_HI | R/W | PCIE_H PHY Hi Configuration Access Register |
| 0x05e0 | PCIE_G0_REG | R/W | PCIE_G0 Configuration Register |

| Address Offset | Name | Read/Write | Description |
|----------------|----------------|------------|--|
| 0x05f0 | PCIE_G0_PHY_LO | R/W | PCIE_G0 PHY Lo Configuration Access Register |
| 0x05f8 | PCIE_G0_PHY_HI | R/W | PCIE_G0 PHY Hi Configuration Access Register |
| 0x0600 | PCIE_G1_REG | R/W | PCIE_G1 Configuration Register |
| 0x0610 | PCIE_G1_PHY_LO | R/W | PCIE_G1 PHY Lo Configuration Access Register |
| 0x0618 | PCIE_G1_PHY_HI | R/W | PCIE_G1 PHY Hi Configuration Access Register |
| 0x0740 | SATA0_REG | R/W | Configuration of SATA0 |
| 0x0748 | SATA0_PHY | R/W | PHY configuration access register for SATA0 |
| 0x0750 | SATA1_REG | R/W | SATA1 configuration |
| 0x0758 | SATA1_PHY | R/W | PHY configuration access register for SATA1 |
| 0x0760 | SATA2_REG | R/W | SATA2 configuration |
| 0x0768 | SATA2_PHY | R/W | SATA2 PHY Configuration Access Register |
| 0x3838 | GMEM_BAR_MASK | R/W | Memory Capacity Configuration Register |
| 0x3ff8 | CHIP_ID | RO | Chip Version Number |

4.1. HT clock enable and DMA routing configuration

Offset Address: 0418-041Bh

Attribute: R/W

Default value: 3h

Size: 32 bits

Table 9. Table ht clock enable

| Bit Field | Name | Read/Write | Description |
|-----------|-------------|------------|---|
| 31:2 | Reserved | R/W | Reserved |
| 1 | ht_hi_clken | R/W | HT Controller 1 Clock Enable 0: Turn off the clock 1: Turn on the clock |
| 0 | ht_lo_clken | R/W | HT Controller 0 Clock Enable 0: Turn off the clock 1: Turn on the clock |

Offset Address: 041C-041Fh

Attribute: R/W

Default value: 000a_a800h

Size: 32 bits

This register is used to configure the routing information for the device's DMA accesses (i.e., the destination processor for the DMA access and the HT controller through which it passes). Since the HT bus only supports 40-bit addresses and the processor space (and the DMA access space) supports 64-bit addresses, the addresses need to be transformed before and after passing through the HT bus in order to preserve the address routing information. This feature requires two supports:

1. the bridge chip stores the node number information in a certain number of bits of the HT bus address;
2. on the processor side, the node information is remapped to the processor's node bit field using the address translation function of the HT receive window.

The LS7A1000 implements the DMA access node number translation function, which allows the node number in the 64-bit address space issued by the device to be automatically mapped to the HT address space by configuring this register.

Table 10. DMA routing configuration

| Bit Field | Name | Read/Write | Description |
|-----------|-------------|------------|--|
| 31:16 | dma_dest_ht | R/W | <p>DMA access destination node routing configuration. There are 16 nodes, each bit corresponds to a node number. bit31-16 correspond to DMA accesses to nodes 15-0 respectively.</p> <p>1: Routed to HT controller 1</p> <p>0: Routed to HT controller 0</p> |

| Bit Field | Name | Read/Write | Description |
|-----------|--|------------|---|
| 15:13 | <code>dma_node_id_offset_mapped</code> | R/W | <p>Address Offset of the mapped DMA access node number in the HT address space (relative to <code>bit32</code>).</p> <p>0: Position of the node number in the HT address space from <code>bit32</code></p> <p>1: Position of the node number in the HT address space from <code>bit33</code></p> <p>...</p> <p>7: The location of the node number in the HT address space starts at <code>bit39</code></p> <p>This register determines the maximum address range for DMA accesses to a single node. For example, when this register is configured to 0 and <code>bit[3:0]</code> is not 0, the maximum address space for DMA accesses within a single node is $2^{32}=4GB$.</p> |
| 12:8 | <code>dma_node_id_offset</code> | R/W | The address offset (relative to <code>bit36</code>) where the node number is located in the DMA access. |
| 7:4 | Reserved | R/W | Reserved |
| 3:0 | <code>dma_node_id_mask</code> | R/W | <p>Node number mask for DMA accesses. This register determines the number of nodes that can be accessed by device DMA access.</p> <p>0 : 1 node</p> <p>1 : 2 nodes</p> <p>3 : 4 nodes</p> <p>7 : 8 nodes</p> <p>15 : 16 nodes</p> |

4.2. General Configuration Register 0

Offset Address: `0420-0423h`

Attribute: R/W

Default value: `CCCC_3CE0h`

Size: **32** bits

This register contains configuration information related to PCIe, graphics processing unit (GPU, display

controller, graphics memory).

Table 11. Table General Configuration Register 0 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------------|------------|---|
| 31 | pcie_g1_p1_clken | R/W | Enables the port1 clock for pcie_g1 0: Turn off the clock 1: Turn on the clock |
| 30 | pcie_g1_p0_clken | R/W | Enables the port0 clock for pcie_g1 0: Turn off the clock 1: Turn on the clock |
| 29 | pcie_g1_enable | R/W | Enable pcie_g1 controller 0: Access is disabled 1: Access is allowed |
| 28 | pcie_g1_soft_reset | R/W | Software reset of pcie_g1 0: Remove reset 1: Hold reset |
| 27 | pcie_g0_p1_clken | R/W | Enables the port1 clock for pcie_g0 0: Turn off the clock 1: Turn on the clock |
| 26 | pcie_g0_p0_clken | R/W | Enables the port0 clock for pcie_g0 0: Turn off the clock 1: Turn on the clock |
| 25 | pcie_g0_enable | R/W | Enable pcie_g0 controller 0: Access is disabled 1: Access is allowed |
| 24 | pcie_g0_soft_reset | R/W | Software reset of pcie_g0 0: Remove reset 1: Hold reset |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------------|------------|---|
| 23 | pcie_h_p1_clken | R/W | Enables the port1 clock for pcie_h 0: Turn off the clock 1: Turn on the clock |
| 22 | pcie_h_p0_clken | R/W | Enables the port0 clock for pcie_h 0: Turn off the clock 1: Turn on the clock |
| 21 | pcie_h_enable | R/W | Enable pcie_h controller 0: Access is disabled 1: Access is allowed |
| 20 | pcie_h_soft_reset | R/W | Software reset of pcie_h 0: Remove reset 1: Hold reset |
| 19 | pcie_f1_p1_clken | R/W | Enables the port1 clock for pcie_f1 0: Turn off the clock 1: Turn on the clock |
| 18 | pcie_f1_p0_clken | R/W | Enables the port0 clock for pcie_f1 0: Turn off the clock 1: Turn on the clock |
| 17 | pcie_f1_enable | R/W | Enable pcie_f1 controller 0: Access is disabled 1: Access is allowed |
| 16 | pcie_f1_soft_reset | R/W | Software reset of pcie_f1 0: Remove reset 1: Hold reset |
| 15:14 | Reserved | R/W | Reserved |
| 13 | pcie_f0_p3_clken | R/W | Enables the port3 clock for pcie_f0 0: Turn off the clock 1: Turn on the clock |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------------|------------|---|
| 12 | pcie_f0_p2_clken | R/W | Enables the port2 clock for pcie_f0 0: Turn off the clock 1: Turn on the clock |
| 11 | pcie_f0_p1_clken | R/W | Enables the port1 clock for pcie_f0 0: Turn off the clock 1: Turn on the clock |
| 10 | pcie_f0_p0_clken | R/W | Enables the port0 clock for pcie_f0 0: Turn off the clock 1: Turn on the clock |
| 9 | pcie_f0_enable | R/W | Enable pcie_f0 controller 0: Access is disabled 1: Access is allowed |
| 8 | pcie_f0_soft_reset | R/W | Software reset of pcie_f0 0: Remove reset 1: Hold reset |
| 7 | dc_clken | R/W | Enables clocking of dc 0: Turn off the clock 1: Turn on the clock |
| 6 | gpu_clken | R/W | Enable the clock of the gpu 0: Turn off the clock 1: Turn on the clock |
| 5 | gmem_clken | R/W | Enables the clock for gmem 0: Turn off the clock 1: Turn on the clock |
| 4:3 | Reserved | R/W | Reserved |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------------|------------|--|
| 2 | pcie_clkssel | R/W | <p>Clock selection for pcie.</p> <p>0: Selects the PAD input clock</p> <p>1: Select the internal reference clock</p> <p>If fix_pcie_clkssel is 1, then the signal is constant to 1.</p> |
| 1 | Reserved | R/W | Reserved |
| 0 | default_route_cfg0 | R/W | <p>Read/Writeing PCIE, graphics devices using fixed addresses. 0: Configuring device addresses using the PCI configuration header</p> <p>1: Use fixed address to access the device</p> <p>If fix_default_route is 1, then the signal is constant to 1.</p> |

Offset Address: 0424-0427h

Attribute: R/W, R0

Default value: 0000_0000h

Size: 32 bits

Table 12. DMA routing configuration

| Bit Field | Name | Read/Write | Description |
|-----------|------------------------|------------|---|
| 31:25 | Reserved | R/W | Reserved |
| 24 | disable_gmem_confspace | R/W | <p>Disable access to the GMEM configuration space</p> <p>0: Access allowed</p> <p>1: Access is prohibited</p> |
| 23:20 | Reserved | R/W | Reserved |
| 19 | pcie_g1_p1_clk_ok | RO | <p>pcie_g1 port 1 clock ready</p> <p>0: No clock</p> <p>1: clock normal</p> |
| 18 | pcie_g1_p0_clk_ok | RO | <p>pcie_g1 port 0 clock ready</p> <p>0: No clock</p> <p>1: clock normal</p> |

| Bit Field | Name | Read/Write | Description |
|-----------|-------------------|------------|--|
| 17 | pcie_g0_p1_clk_ok | RO | pcie_g0 port 1 clock ready 0: No clock 1: clock normal |
| 16 | pcie_g0_p0_clk_ok | RO | pcie_g0 port 0 clock ready 0: No clock 1: clock normal |
| 15 | pcie_h_p1_clk_ok | RO | pcie_h port 1 clock ready 0: No clock 1: clock normal |
| 14 | pcie_h_p0_clk_ok | RO | pcie_h port 0 clock ready 0: No clock 1: clock normal |
| 13 | pcie_f1_p1_clk_ok | RO | pcie_f1 port 1 clock ready 0: No clock 1: clock normal |
| 12 | pcie_f1_p0_clk_ok | RO | pcie_f1 port 0 clock ready 0: No clock 1: clock normal |
| 11 | pcie_f0_p0_clk_ok | RO | pcie_f0 port 3 clock ready 0: No clock 1: clock normal |
| 10 | pcie_f0_p0_clk_ok | RO | pcie_f0 port 2 clock ready 0: No clock 1: clock normal |
| 9 | pcie_f0_p0_clk_ok | RO | pcie_f0 port 1 clock ready 0: No clock 1: clock normal |

| Bit Field | Name | Read/Write | Description |
|-----------|-------------------|------------|--|
| 8 | pcie_f0_p0_clk_ok | RO | pcie_f0 port 0 clock ready 0: No clock 1: clock normal |
| 5 | pcie_g1_uca_en | R/W | pcie_g1 uncached access acceleration enable 0: Turn off access acceleration 1: Turn on access acceleration |
| 4 | pcie_g0_uca_en | R/W | pcie_g0 uncached access acceleration enable 0: Turn off access acceleration 1: Turn on access acceleration |
| 3 | pcie_h_uca_en | R/W | pcie_h uncached access acceleration enable 0: Turn off access acceleration 1: Turn on access acceleration |
| 2 | pcie_f1_uca_en | R/W | pcie_f1 uncached access acceleration enable 0: Turn off access acceleration 1: Turn on access acceleration |
| 1 | pcie_f0_uca_en | R/W | pcie_f0 uncached access acceleration enable 0: Turn off access acceleration 1: Turn on access acceleration |
| 0 | graphic_uca_en | R/W | GPU/DC uncached access acceleration can be 0: Turn off access acceleration 1: Turn on access acceleration |

4.3. General Configuration Register 1

Offset Address: 0430-0433h

Attribute: R/W

Default value: 00F9_BBF2h

Size: 32 bits

This register contains configuration information related to USB, SATA, GMAC, HDA/AC97, LPC, and SPI.

Table 13. Table general configuration register 0 2

| Bit Field | Name | Read/Write | Description |
|-----------|-------------|------------|---|
| 31 | lpc_uca_en | R/W | LPC uncache acceleration enable 0: turn off access acceleration 1: Turn on access acceleration |
| 30 | spi_uca_en | R/W | SPI uncache acceleration enable 0: Turn off access acceleration 1: Access acceleration on |
| 29 | conf_uca_en | R/W | Configuration register uncache acceleration enable 0: Turn off access acceleration 1: turn on access acceleration |
| 28 | misc_uca_en | R/W | Low-speed misc device uncache acceleration enable 0: turn off access acceleration 1: turn on access acceleration |
| 27 | aud_uca_en | R/W | HDA/AC97 uncache acceleration enable 0: Turn off access acceleration 1: Turn on access acceleration |
| 26 | gmac_uca_en | R/W | gmac uncache acceleration enable 0: Turn off access acceleration 1: Turn on access acceleration |
| 25 | sata_uca_en | R/W | sata uncache acceleration enable 0: turn off access acceleration 1: Turn on access acceleration |
| 24 | usb_uca_en | R/W | usb uncache acceleration enable 0: turn off access acceleration 1: Turn on access acceleration |
| 23:16 | Reserved | R/W | Reserved |

| Bit Field | Name | Read/Write | Description |
|-----------|----------------------|------------|--|
| 15 | usb1_clken | R/W | usb1 clock enable 0: No clock 1: clock normal |
| 14 | usb1_en | R/W | usb_1 access enable 0: Access disabled 1: Access allowed |
| 13 | usb1_phy_soft_reset | R/W | usb1 PHY software reset 0: Remove reset 1: Hold reset |
| 12 | usb1_cntl_soft_reset | R/W | usb1 controller software reset 0: Remove reset 1: Hold reset |
| 11 | usb0_clken | R/W | usb0 clock enable 0: No clock 1: clock normal |
| 10 | usb0_en | R/W | usb0 access enable 0: Access disabled 1: Access allowed |
| 9 | usb0_phy_soft_reset | R/W | usb0 PHY software reset 0: Remove reset 1: Hold reset |
| 8 | usb0_cntl_soft_reset | R/W | usb0 controller software reset 0: Remove reset 1: Hold reset |
| 7 | gmac1_clken | R/W | gmac1 clock enable 0: No clock 1: clock normal |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------------|------------|---|
| 6 | gmac1_sdb_flowctrl | R/W | gmac1 flow control enable 0 : Flow control off 1 : Flow control on |
| 5 | gmac0_clken | R/W | gmac0 clock enable 0 : No clock 1 : clock normal |
| 4 | gmac0_sdb_flowctrl | R/W | gmac0 flow control enable 0 : Flow control off 1 : Flow control on |
| 3:2 | usb_ref_clk_sel | R/W | USB PHY Reference Clock Selection 00b : Use external 12MHz crystal 10b : Use internal reference clock |
| 1 | usb_ehci_dma64_en | R/W | Enables usb EHCI 64 -bit DMA address mode 0 : Use 32 -bit DMA address mode 1 : Use 64 -bit DMA address mode |
| 0 | default_route_cfg1 | R/W | Use fixed addresses to access devices such as USB , SATA , GMAC , etc. 0 : Use the PCI configuration header to configure the device address 1 : Use fixed address to access the device If fix_default_route is 1 , then the signal is constant to 1 . |

Note: In order to support the USB sleep-wake function, the USB reference clock must use a 12MHz external crystal.

Offset Address: **0430-0437h**

Attribute: R/W

Default value: **1209_9900h**

Size: **32** bits

Table 14. Table general configuration register 0 3

| Bit Field | Name | Read/Write | Description |
|-----------|------------------------------------|------------|---|
| 28 | <code>hda_dma_64</code> | R/W | Enables HDA64 bit DMA address mode 0: Use 32 -bit DMA address mode 1: Use 64 -bit DMA address mode |
| 27 | <code>rtc_restart</code> | R/W | RTC crystal oscillator restart |
| 26:24 | <code>rtc_ds</code> | R/W | RTC Crystal Oscillator Driver Configuration |
| 19 | <code>sata2_clk_en</code> | R/W | SATA2 clock enable 0: No clock 1: Normal clock |
| 18 | <code>sata2_en</code> | R/W | SATA2 access enable 0: Access disabled 1: Access allowed |
| 16 | <code>sata2_cntl_soft_reset</code> | R/W | SATA2 controller software reset 0: Remove reset 1: Hold reset |
| 15 | <code>sata1_clken</code> | R/W | SATA1 clock enable 0: No clock 1: Clock normal |
| 14 | <code>sata1_en</code> | R/W | SATA1 access enable 0: Access disabled 1: Access allowed |
| 12 | <code>sata1_cntl_soft_reset</code> | R/W | SATA1 controller software reset 0: Remove reset 1: Hold reset |
| 11 | <code>sata0_clken</code> | R/W | SATA0 clock enable 0: No clock 1: Clock normal |

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------------|------------|--|
| 10 | sata0_en | R/W | SATA0 Access Enable 0 : Access disabled 1 : Access allowed |
| 8 | sata0_cntl_soft_reset | R/W | SATA0 Controller software reset 0 : Remove reset 1 : Hold Reset 7:1 Reserved R/W Reserved |
| 0 | lpc_en | R/W | LPC controller enable 0 : Access is disabled 1 : Access allowed |

4.4. Pin Multiplexing Configuration Register

Offset Address: 0440-0443h

Attribute: R/W

Default value: FFFF_FFFFh

Size: 32 bits

This register contains configuration information related to pin multiplexing.

Table 15. Pin multiplexing configuration register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31 | uart3_enable | R/W | UART operating mode selection for pin UART_RI/DCD (when selected as UART mode) 0 : use or not is determined by bit28 1 : Operates in two-wire UART3 mode |
| 30 | uart2_enable | R/W | UART operating mode selection for pin UART_DTR/DSR (when selected as UART mode) 0 : use or not is determined by bit28 1 : Operates in two-wire UART2 mode |

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------------|------------|---|
| 29 | uart1_enable | R/W | <p>UART operating mode selection for pin UART_RTS/CTS (when selected as UART mode)</p> <p>0: use or not is determined by bit28</p> <p>1: Operates in two-wire UART1 mode</p> |
| 28 | uart0_full_func | R/W | <p>UART operating mode selection for pin UART_TXD/RXD (when UART mode is selected)</p> <p>0: Operates in two-wire UART0 mode</p> <p>1: Working in full-function UART0 mode</p> <p>When bit[31:29] is not equal to 0, regardless of the value of this bit, UART_TXD/RXD operates in two-wire UART mode regardless of the value of the bit.</p> |
| 27 | clkoutflex_sel | R/W | <p>Operating mode selection for pin CLKOUTFLEX</p> <p>0: working in GPIO mode</p> <p>1: Operates in CLKOUTFLEX mode</p> |
| 26 | clkout25m_sel | R/W | <p>Operating mode selection for pin CLKOUT25M</p> <p>0: working in GPIO mode</p> <p>1: Operating in CLKOUT25M mode</p> |
| 25 | lpc_sel | R/W | <p>Operating mode selection for LPC pins (LPC_AD0-3/LPC_SERIRQ/LPC_FRAMEn)</p> <p>0: working in GPIO mode</p> <p>1: Working in LPC mode</p> |
| 24 | uart_dtr_dsr_sel_i2 c | R/W | <p>Operating mode selection for pin UART_DTR/DSR (determined together with bit20)</p> <p>[bit24, bit20].</p> <p>00b: working in GPIO mode</p> <p>x1b: working in UART mode (decided by bit[31:28] whether to work in full function mode)</p> <p>10b: working in I2C mode</p> |

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------------|------------|--|
| 23 | uart_ri_dcd_sel_i2c | R/W | <p>Operating mode selection for pin UART_RI/DCD (determined together with bit19)</p> <p>[bit23, bit19].</p> <p>00b: working in GPIO mode</p> <p>x1b: working in UART mode (decided by bit[31:28] whether to work in full function mode)</p> <p>10b: working in I2C mode</p> |
| 22 | uart_txd_rxd_sel_uart | R/W | <p>Operating mode selection for pin UART_TXD/RXD</p> <p>0: working in GPIO mode</p> <p>1: working in UART mode (the bit[31:28] determines whether to work in full function mode)</p> |
| 21 | uart_rts_cts_sel_uart | R/W | <p>Operating mode selection for pin UART_RTS/CTS</p> <p>0: working in GPIO mode</p> <p>1: working in UART mode (determined by bit[31:28] whether to work in full function mode)</p> |
| 20 | uart_dtr_dsr_sel_uart | R/W | <p>Operating mode selection for pin UART_DTR/DSR (determined together with bit24)</p> <p>[bit24, bit20].</p> <p>00b: working in GPIO mode</p> <p>x1b: working in UART mode (decided by bit[31:28] whether to work in full function mode)</p> <p>10b: working in I2C mode</p> |

| Bit Field | Name | Read/Write | Description |
|-----------|----------------------|------------|--|
| 19 | uart_ri_dcd_sel_uart | R/W | Operating mode selection for pin UART_RI/DCD (determined together with bit23) [bit23, bit19]. 00b: working in GPIO mode x1b: working in UART mode (decided by bit[31:28] whether to work in full function mode) 10b: working in I2C mode |
| 18 | usb_oc2_sel | R/W | Operating mode selection for pin USB_OC2 0: working in GPIO mode 1: Working in USB_OC mode |
| 17 | usb_oc1_sel | R/W | Operating mode selection for pin USB_OC1 0: working in GPIO mode 1: Working in USB_OC mode |
| 16 | usb_oc0_sel | R/W | Operating mode selection for pin USB_OC0 0: working in GPIO mode 1: working in USB_OC mode |
| 15 | sata2_ledn_sel | R/W | Operating mode selection for pin SATA2_LEDn 0: working in GPIO mode 1: Operates in SATA mode |
| 14 | sata1_ledn_sel | R/W | Operating mode selection for pin SATA1_LEDn 0: working in GPIO mode 1: Operates in SATA mode |
| 13 | sata0_ledn_sel | R/W | Operating mode selection for pin SATA0_LEDn 0: working in GPIO mode 1: Operates in SATA mode |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------------|------------|--|
| 12:11 | hda_ac97_sel | R/W | <p>Operating mode selection for HDA pins. For the pins</p> <p>HDA_BITCLK/HDA_SYNC/HDA_RESETn/HDA_SDO/HDA_SDI0, the operating mode is determined by bit[12:11]:</p> <ul style="list-style-type: none"> 00b: GPIO mode 10b: AC97 mode x1b: HDA mode <p>For pins HDA_SDI1/HDA_SDI2, the operating mode is determined by bit[11]:</p> <ul style="list-style-type: none"> 0: GPIO mode 1: HDA mode |
| 10 | spi_sel | R/W | <p>Operating mode selection for pin SPI_SCK/SDI/SDO</p> <ul style="list-style-type: none"> 0: Operates in GPIO mode 1: Operates in SPI mode |
| 9:8 | spi_csn_23_sel_spi | R/W | <p>Operating mode selection for pin SPI_CSn2/3</p> <ul style="list-style-type: none"> 00b: operates in GPIO mode x1b: working in SPI mode 10b: Operating in I2C mode |
| 7:6 | spi_csn_01_sel_spi | R/W | <p>Operating mode selection for pin SPI_CSn0/1</p> <ul style="list-style-type: none"> 00b: Operates in GPIO mode x1b: working in SPI mode 10b: Operating in I2C mode |
| 5 | i2c1_sel | R/W | <p>Operating mode selection for pin I2C1_SCL/SDA</p> <ul style="list-style-type: none"> 0: working in GPIO mode 1: Working in I2C mode |
| 4 | i2c0_sel | R/W | <p>Operating mode selection for pin I2C0_SCL/SDA</p> <ul style="list-style-type: none"> 0: working in GPIO mode 1: Working in I2C mode |

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|--|
| 3 | pwm3_sel | R/W | Operating mode selection for pin PWM3 0: Operates in GPIO mode 1: Operates in PWM mode |
| 2 | pwm2_sel | R/W | Operating mode selection for pin PWM2 0: Operates in GPIO mode 1: Operates in PWM mode |
| 1 | pwm1_sel | R/W | Operating Mode Selection for Pin PWM1 0: Operates in GPIO mode 1: Operates in PWM mode |
| 0 | pwm0_sel | R/W | Operating mode selection for pin PWM0 0: Operates in GPIO mode 1: Operates in PWM mode |

The multiplexing relationship between the VSB_GATEn pin and GPIO01 is configured by the internal register (PMCON_RESUME) of the power management module, see 12.3 Register Description.

See the chip pin multiplexing table in Appendix 1 for a cross-reference to the chip pin multiplexing table.

4.5. PLL0 Configuration Register

Please refer to Section 2.5 PLL Configuration Method for the specific usage of PLL. This register is used to set PLL0, where output clock 1 is used to generate the 125MHz clock required by the GMAC, and output clock 0

is used to generate the controller clock for USB/SATA.

Offset Address: 0480-0483h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

This register contains configuration information related to pin multiplexing.

Table 16. PLL0 configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|------------------------------|
| 31:30 | Reserved | R/W | Reserved |
| 29:21 | pll_loopc | R/W | PLL Multiplier |
| 20:14 | pll_div_out2 | R/W | PLL output clock 2 divisions |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|------------------------------|
| 13:7 | pll_div_out1 | R/W | PLL output clock 1 division |
| 6:0 | pll_div_out0 | R/W | PLL output clock 0 divisions |

Offset Address: 0484-0487h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 17. PLL0 configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|-------------------------------------|
| 31:14 | Reserved | R/W | Reserved |
| 13 | pll_pd | R/W | PLL powerdown |
| 12 | pll_bypass | R/W | PLL internal bypass |
| 11 | set_pll_param | R/W | Set PLL configuration parameters |
| 10 | sel_pll_out2 | R/W | Select PLL output clock 2 |
| 9 | sel_pll_out1 | R/W | Select PLL output clock 1 |
| 8 | sel_pll_out0 | R/W | Select PLL Output Clock 0 |
| 7 | pll_locked | RO | PLL Lock |
| 6:0 | pll_div_ref | R/W | PLL Input Frequency Division Number |

4.6. PLL1 Configuration Register

Please refer to Section 2.5 PLL Configuration Method for the specific usage of PLL.

This register is used to set PLL1, where output clock 2 is used to generate the GPU clock, output clock 1 is used to generate the GMEM clock, and output clock 0 is used to generate the DC clock.

Offset Address: 0490-0493h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 18. PLL1 configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|------------------------------|
| 31:30 | Reserved | R/W | Reserved |
| 29:21 | pll_loopc | R/W | PLL Multiplier |
| 20:14 | pll_div_out2 | R/W | PLL output clock 2 divisions |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|------------------------------|
| 13:7 | pll_div_out1 | R/W | PLL output clock 1 division |
| 6:0 | pll_div_out0 | R/W | PLL output clock 0 divisions |

Offset Address: 0494-0497h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 19. PLL1 configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|-------------------------------------|
| 31:14 | Reserved | R/W | Reserved |
| 13 | pll_pd | R/W | PLL powerdown |
| 12 | pll_bypass | R/W | PLL internal bypass |
| 11 | set_pll_param | R/W | Set PLL configuration parameters |
| 10 | sel_pll_out2 | R/W | Select PLL output clock 2 |
| 9 | sel_pll_out1 | R/W | Select PLL output clock 1 |
| 8 | sel_pll_out0 | R/W | Select PLL Output Clock 0 |
| 7 | pll_locked | RO | PLL Lock |
| 6:0 | pll_div_ref | R/W | PLL Input Frequency Division Number |

4.7. PLL2 Configuration Register

Please refer to Section 2.5 PLL Configuration Method for the specific usage of PLL. This register is used to set PLL2, where output clock 2 is used to generate the CLKOUTFLEX clock, output clock 1 is used to generate the internal bus clock, and output clock 0 is used to generate the 24MHz bitclk clock required by the HDA.

Output Clock 1 is used to generate the internal bus clock, and Output Clock 0 is used to generate the 24MHz bitclk clock required by the HDA.

Address Offset: 04A0-04A3h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 20. PLL2 configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|----------------|
| 31:30 | Reserved | R/W | Reserved |
| 29:21 | pll_loopc | R/W | PLL Multiplier |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|------------------------------|
| 20:14 | pll_div_out2 | R/W | PLL output clock 2 divisions |
| 13:7 | pll_div_out1 | R/W | PLL output clock 1 division |
| 6:0 | pll_div_out0 | R/W | PLL output clock 0 divisions |

Address Offset: 04A4-04A7h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 21. PLL2 configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|-------------------------------------|
| 31:14 | Reserved | R/W | Reserved |
| 13 | pll_pd | R/W | PLL powerdown |
| 12 | pll_bypass | R/W | PLL internal bypass |
| 11 | set_pll_param | R/W | Set PLL configuration parameters |
| 10 | sel_pll_out2 | R/W | Select PLL output clock 2 |
| 9 | sel_pll_out1 | R/W | Select PLL output clock 1 |
| 8 | sel_pll_out0 | R/W | Select PLL Output Clock 0 |
| 7 | pll_locked | RO | PLL Lock |
| 6:0 | pll_div_ref | R/W | PLL Input Frequency Division Number |

4.8. PLL_PIX_0 Configuration Register

Refer to Section 2.5 PLL Configuration Methods for the specific usage of the PLL.

This register is used to set PLL_PIX_0, where output clock 0 is used to generate the PIX0 clock.

Address Offset: 04B0-04B3h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 22. PLL pix 0 configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|----------------|
| 31:30 | Reserved | R/W | Reserved |
| 29:21 | pll_loopc | R/W | PLL Multiplier |
| 20:7 | Reserved | R/W | Reserved |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|----------------------------|
| 6:0 | pll_div_out0 | R/W | PLL Output Clock 0 Divider |

Address Offset: 04B4-04B7h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 23. PLL pix 0 configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|----------------------------------|
| 31:14 | Reserved | R/W | Reserved |
| 13 | pll_pd | R/W | PLL powerdown |
| 12 | pll_bypass | R/W | PLL internal bypass |
| 11 | set_pll_param | R/W | Set PLL configuration parameters |
| 10:9 | Reserved | R/W | Reserved |
| 8 | sel_pll_out0 | R/W | Select PLL output clock 0 |
| 7 | pll_locked | RO | PLL Lock |
| 6:0 | pll_div_ref | R/W | Number of PLL input divisions |

4.9. PLL_PIX_1 Configuration Register

Refer to Section 2.5 PLL Configuration Methods for the specific usage of the PLL. This register is used to set PLL_PIX_1, where output clock 0 is used to generate the PIX1 clock.

Address Offset: 04C0-04C3h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 24. PLL_PIX_1 Configuration Register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|----------------------------|
| 31:30 | Reserved | R/W | Reserved |
| 29:21 | pll_loopc | R/W | PLL Multiplier |
| 20:7 | Reserved | R/W | Reserved |
| 6:0 | pll_div_out0 | R/W | PLL Output Clock 0 Divider |

Address Offset: 04C4-04C7h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 25. PLL_PIX_1 Configuration Register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|----------------------------------|
| 31:14 | Reserved | R/W | Reserved |
| 13 | pll_pd | R/W | PLL powerdown |
| 12 | pll_bypass | R/W | PLL internal bypass |
| 11 | set_pll_param | R/W | Set PLL configuration parameters |
| 10:9 | Reserved | R/W | Reserved |
| 8 | sel_pll_out0 | R/W | Select PLL output clock 0 |
| 7 | pll_locked | RO | PLL lockout |
| 6:0 | pll_div_ref | R/W | Number of PLL input divisions |

4.10. PCIE_F0 PHY Configuration Register

This set of registers contains the control signals for PCIE_F0 PHY.

Address Offset: 0588-058Bh

Attribute: R/W, RO

Default value: 0006_0000h

Size: 32 bits

Table 26. Pcie f0 phy configuration register

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|--|
| 27 | cfg_x4_mode_en | R/W | Enable software to configure the operating mode of PCIE_F0 0: the operating mode is determined by the hardware pin 1: The operating mode is determined by the software configuration (bit26) |
| 26 | cfg_x4_mode | R/W | Software configuration of PCIE_F0 operating modes 0: working in x1 mode 1: working in x4 mode |
| 24 | phy_powerdown | R/W | Set PHY into low-power mode |

4.11. PCIE_F0 PHY Access Configuration Register

This group of registers is used to control the configuration access operation that generates the PCIE_F0 PHY internal control register. This register controls the 4 data links of PCIE_F0.

Address Offset: 0590-0593h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 27. PCIE_F0 PHY Access Configuration Register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:16 | phy_cfg_data | R/W | PHY configuration reads and writes data. In the write operation, the data is written to this register before the write operation is executed; in the read operation, the read data returned from PHY is stored to this register. |
| 15:0 | phy_cfg_addr | R/W | PHY configures the address. |

Address Offset: 0594-0597h

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 28. PCIE_F0 PHY Access Configuration Register 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |
| 2 | phy_cfg_done | R/W | PHY One access completion indicates the completion of reading and writing to PHY. Write completion indicates that the write data has been written to the PHY internal register, and read completion indicates that the read data has been returned to the phy_cfg_data register |
| 1 | phy_cfg_disable | R/W | 0 - Read and write to this set of registers will trigger PHY configuration access operation 1 - Read or write to this set of registers does not trigger PHY configuration access operation, only a simple register read or write |
| 0 | phy_cfg_R/W | R/W | Start a read operation or a write operation. 0: Read operation 1: Write operation |

4.12. PCIE_F1 PHY Configuration Register

This set of registers contains the control signals for PCIE_F1 PHY.

Address Offset: 05A8-05ABh

Attribute: R/W, R0

Default value: 0006_0000h

Size: 32 bits

Table 29. PCIE_F1 PHY Configuration Register 1

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|--|
| 27 | cfg_x4_mode_en | R/W | Enable software to configure the operating mode of PCIE_F1 0: the operating mode is determined by the hardware pin 1: The operating mode is determined by the software configuration (bit26) |
| 26 | cfg_x4_mode | R/W | Software configuration of PCIE_F1 operating modes 0: working in x1 mode 1: working in x4 mode |
| 24 | phy_powerdown | R/W | Set PHY into low-power mode |

4.13. PCIE_F1 PHY Access Configuration Register

This group of registers is used to control the configuration access operation that generates the PCIE_F1 PHY internal control register. This register controls the 4 data links of PCIE_F1.

Address Offset: 05B0-05B3h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 30. pcie f1 phy access configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:16 | phy_cfg_data | R/W | PHY configuration reads and writes data. In the write operation, the data is written to this register first, and then the write operation is performed. In the read operation, the read data returned from PHY is stored into this register. |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---------------------------|
| 15:0 | phy_cfg_addr | R/W | PHY configuration address |

Address Offset: 05B4-05B7h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 31. pcie f1 phy access configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |
| 2 | phy_cfg_done | R/W | The completion of one access to PHY indicates the completion of reading and writing to PHY. Write completion indicates that the written data has been written to the PHY internal register, and read completion indicates that the read data has been returned to the phy_cfg_data register |
| 1 | phy_cfg_disable | R/W | 0 - Read or write to this group of registers will trigger the PHY configuration access operation 1 - Read or write to this set of registers does not trigger PHY configuration access operation, only a simple register read or write |
| 0 | phy_cfg_R/W | R/W | Start a read operation or a write operation. 0: Read operation 1: Write operation |

4.14. PCIE_H PHY Configuration Register

This group of registers contains the control signals for PCIE_H PHY.

Address Offset: 05C8-05CBh

Attribute: R/W, RO

Default value: 0006_0000h

Size: 32 bits

Table 32. Pcie h phy configuration register

| Bit Field | Name | Read/Write | Description |
|-----------|------------------|------------|--|
| 27 | cfg_x4_mode_en | R/W | Enable software to configure the operating mode of PCIE_H 0: the operating mode is determined by the hardware pins 1: The operating mode is determined by the software configuration (bit26) |
| 26 | cfg_x4_mode | R/W | Software configuration of PCIE_H operating modes 0: working in x8 mode 1: working in x4 mode |
| 25 | phy_powerdown_hi | R/W | Set the high four bits of PHY to enter the low-power mode |
| 24 | phy_powerdown_lo | R/W | Set PHY low four bits to enter low-power mode |

4.15. PCIE_H PHY LO Access Configuration Register

This group of registers is used to control the configuration access operation that generates the PCIE_H PHY LO internal control register. This register controls the the lower 4 data links (lane0-3) of PCIE_H.

Address Offset: 05D0-05D3h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 33. Pcie h phy lo access configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:16 | phy_cfg_data | R/W | PHY configuration reads and writes data. In the write operation, the data is written to this register first, and then the write operation is performed. In the read operation, the read data returned from PHY is stored into this register. |
| 15:0 | phy_cfg_addr | R/W | PHY Configuration Address |

Address Offset: 05D4-05D7h

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 34. Pcie h phy lo access configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |
| 2 | phy_cfg_done | R/W | The completion of one access to PHY indicates the completion of reading and writing to PHY. Write completion indicates that the written data has been written to the PHY internal register, and read completion indicates that the read data has been returned to the phy_cfg_data register |
| 1 | phy_cfg_disable | R/W | 0 - Read or write to this group of registers will trigger the PHY configuration access operation 1 - Read or write to this set of registers does not trigger PHY configuration access operation, only a simple register read or write |
| 0 | phy_cfg_R/W | R/W | Start a read operation or a write operation. 0: Read operation 1: Write operation |

4.16. PCIE_H PHY HI Access Configuration Register

This group of registers is used to control the configuration access operation that generates the PCIE_H PHY HI internal control register. This register controls the the high 4 data links (lane4-7) of PCIE_H.

Address Offset: 05D8-05DBh

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 35. Pcie h phy hi access configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 31:16 | phy_cfg_data | R/W | PHY configures the read and write data. In the write operation, the data is written to this register before the write operation is executed; in the read operation, the read data returned from PHY is stored to this register. |
| 15:0 | phy_cfg_addr | R/W | PHY Configuration Address |

Address Offset: 05DC-05DFh

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 36. Pcie h phy hi access configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |
| 2 | phy_cfg_done | R/W | The completion of one access to PHY indicates the completion of reading and writing to PHY. Write completion indicates that the written data has been written to the PHY internal register, and read completion indicates that the read data has been returned to the phy_cfg_data register |
| 1 | phy_cfg_disable | R/W | 0 - Read or write to this group of registers will trigger the PHY configuration access operation 1 - Read or write to this set of registers does not trigger PHY configuration access operation, only a simple register read or write |
| 0 | phy_cfg_R/W | R/W | Start a read operation or a write operation. 0: Read operation 1: Write operation |

4.17. PCIE_G0 PHY Configuration Register

This set of registers contains the control signals for PCIE_G0 PHY.

Address Offset: 05E8-05EBh

Attribute: R/W, RO

Default value: 0006_0000h

Size: 32 bits

Table 37. Pcie g0 phy configuration register

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|--|
| 27 | cfg_x4_mode_en | R/W | Enables software to configure the operating mode of PCIE_G0 0: the operating mode is determined by the hardware pins 1: The operating mode is determined by the software configuration (bit26) |

| Bit Field | Name | Read/Write | Description |
|-----------|------------------|------------|---|
| 26 | cfg_x4_mode | R/W | Software configuration of PCIE_G0 operating modes 0: working in x8 mode 1: working in x4 mode |
| 25 | phy_powerdown_hi | R/W | Set the high four bits of PHY to enter the low-power mode |
| 24 | phy_powerdown_lo | R/W | Set PHY low four bits to enter low-power mode |

4.18. PCIE_G0 PHY LO Access Configuration Register

This group of registers is used to control the configuration access operation that generates the PCIE_G0 PHY LO internal control register. This register controls the the lower 4 data links (lane0-3) of PCIE_G0.

Address Offset: 05F0-05F3h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 38. Pcie g0 phy lo access configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:16 | phy_cfg_data | R/W | PHY configuration reads and writes data. In the write operation, the data is written to this register first, and then the write operation is performed. In the read operation, the read data returned from PHY is stored into this register. |
| 15:0 | phy_cfg_addr | R/W | PHY Configuration Address |

Address Offset: 05F4-05F7h

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 39. Pcie g0 phy lo access configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|--|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 2 | phy_cfg_done | R/W | PHY One access completion indicates the completion of this read/write to the PHY. Write completion indicates that the write indicates that the read data has been written to the internal register of PHY, and the read completion indicates that the read data has been returned to the phy_cfg_data register. |
| 1 | phy_cfg_disable | R/W | 0 - Read or write to this group of registers will trigger the PHY configuration access operation 1 - Read or write to this set of registers does not trigger PHY configuration access operation, only a simple register read or write |
| 0 | phy_cfg_R/W | R/W | Start a read operation or a write operation. 0: Read operation 1: Write operation |

4.19. PCIE_G0 PHY HI Access Configuration Register

This group of registers is used to control the configuration access operation that generates the PCIE_G0 PHY HI internal control register. This register controls the the high 4 data links (lane4-7) of PCIE_G0.

Address Offset: 05F8-05FBh

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 40. Pcie g0 phy hi access configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:16 | phy_cfg_data | R/W | PHY configuration reads and writes data. In the write operation, the data is written to this register first, and then the write operation is performed. In the read operation, the read data returned from PHY is stored into this register. |
| 15:0 | phy_cfg_addr | R/W | PHY configuration address |

Address Offset: 05FC-05FFh

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 41. Pcie g0 phy hi access configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|--|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |
| 2 | phy_cfg_done | R/W | The completion of one access to PHY indicates the completion of reading and writing to PHY. Write completion indicates that the written data has been written to the PHY internal register, and read completion indicates that the read data has been returned to the to the phy_cfg_data register |
| 1 | phy_cfg_disable | R/W | 0 - Read or write to this set of registers will trigger the PHY configuration access operation 1-Writes and writes to this set of registers do not trigger a PHY configuration access operation, only a simple register register read/write |
| 0 | phy_cfg_R/W | R/W | Start a read operation or a write operation. 0: Read operation 1: Write operation |

4.20. PCIE_G1 PHY Configuration Register

This set of registers contains the control signals for PCIE_G1 PHY.

Address Offset: 0608-060Bh

Attribute: R/W, RO

Default value: 0006_0000h

Size: 32 bits

Table 42. PCIE_G1 PHY configuration register

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 31:30 | Reserved | R/W | Reserved |

| Bit Field | Name | Read/Write | Description |
|-----------|------------------|------------|---|
| 27 | cfg_x4_mode_en | R/W | Enable software to configure the operating mode of PCIE_G1 0: the operating mode is determined by the hardware pins 1: The operating mode is determined by the software configuration (bit26) |
| 26 | cfg_x4_mode | R/W | Software configuration of PCIE_G1 operating modes 0: working in x8 mode 1: working in x4 mode |
| 25 | phy_powerdown_hi | R/W | Set the high four bits of PHY to enter the low-power mode |
| 24 | phy_powerdown_lo | R/W | Set PHY low four bits to enter low-power mode |

4.21. PCIE_G1 PHY LO Access Configuration Register

This group of registers is used to control the configuration access operation that generates the PCIE_G1 PHY LO internal control register. This register controls the the lower 4 data links (lane0-3) of PCIE_G1.

Address Offset: 0610-0613h

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 43. PCIE_G1 PHY LO access configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:16 | phy_cfg_data | R/W | PHY configuration reads and writes data. In the write operation, the data is written to this register first, and then the write operation is performed. In the read operation, the read data returned from PHY is stored into this register. |
| 15:0 | phy_cfg_addr | R/W | PHY Configuration Address |

Address Offset: 0614-0617h

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 44. PCIE_G1 PHY LO access configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |
| 2 | phy_cfg_done | R/W | PHY One Access Complete indicates that the read or write to the PHY is complete. Write completion indicates that the write Read completion indicates that the read data has been returned to the phy_cfg_data register. |
| 1 | phy_cfg_disable | R/W | 0 - Read or write to this group of registers will trigger the PHY configuration access operation 1 - Reading or writing to this set of registers does not trigger a PHY configuration access operation, only a simple register read or write |
| 0 | phy_cfg_R/W | | R/W |

4.22. PCIE_G1 PHY HI Access Configuration Register

This group of registers is used to control the configuration access operation that generates the PCIE_G1 PHY HI internal control register. This register controls the high 4 data links (lane4-7) of PCIE_G1.

Address Offset: 0618-061Bh

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 45. PCIE_G1 PHY HI access configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 31:16 | phy_cfg_data | R/W | PHY configures the read and write data. In the write operation, the data is written to this register before the write operation is executed; in the read operation, the read data returned from PHY is stored to this register. |
| 15:0 | phy_cfg_addr | R/W | PHY Configuration Address |

Address Offset: 061C-061Fh

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 46. PCIE_G1 PHY HI access configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |
| 2 | phy_cfg_done | R/W | The completion of one access to PHY indicates the completion of reading and writing to PHY. Write completion indicates that the written data has been written to the PHY internal register, and read completion indicates that the read data has been returned to the phy_cfg_data register |
| 1 | phy_cfg_disable | R/W | <p>0 - Read or write to this group of registers will trigger the PHY configuration access operation</p> <p>1 - Read or write to this set of registers does not trigger PHY configuration access operation, only a simple register read or write</p> |
| 0 | phy_cfg_R/W | R/W | <p>Start a read operation or a write operation.</p> <p>0: Read operation</p> <p>1: Write operation</p> |

4.23. SATA0 PHY Configuration Register

This register is used to configure some control parameters of SATA0 PHY.

Address Offset: 0740-0743h

Attribute: R/W

Default value: FF9F_0403h

Size: 32 bits

Table 47. SATA0 PHY Configuration Register 1

| Bit Field | Name | Read/Write | Description |
|-----------|-------------|------------|--|
| 3 | Port_reset | R/W | Link Reset |
| 2 | PHY_reset | R/W | PHY Software Reset 0:Unreset 1: Hold reset |
| 1 | ref_use_pad | R/W | <p>PHY Reference Clock Selection</p> <p>0: Use internal reference clock</p> <p>1: Use external reference clock</p> |
| 0 | Reserved | R/W | Reserved |

Address Offset: 0744-0747h

Attribute: R/W

Default value: 7FFF_FFFFh

Size: 32 bits

Table 48. SATA0 PHY Configuration Register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---------------|
| 31 | Phy_power_down | R/W | PHY Powerdown |

4.24. SATA0 PHY Access Configuration Register

This group of registers is used to control the generation of configuration access operations to the SATA0 PHY internal control registers.

Address Offset: 0748-074Bh

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 49. SATA0 PHY Access Configuration Register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:16 | phy_cfg_data | R/W | PHY configuration reads and writes data. In the write operation, the data is written to this register first, and then the write operation is performed. In the read operation, the read data returned from PHY is stored into this register. |
| 15:0 | phy_cfg_addr | R/W | PHY configuration address |

Address Offset: 074C-074Fh

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 50. SATA0 PHY Access Configuration Register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|--|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 2 | phy_cfg_done | R/W | The completion of one access to PHY indicates the completion of reading and writing to PHY. Write completion indicates that the written data has been written to the PHY internal register, and read completion indicates that the read data has been returned to the phy_cfg_data register |
| 1 | phy_cfg_disable | R/W | 0 - Reading or writing to this set of registers triggers a PHY configuration access operation 1 - Reading or writing to this set of registers does not trigger a PHY configuration access operation, but rather acts as a read or write operation to this register |
| 0 | phy_cfg_R/W | R/W | Start a read operation or a write operation. 0: Read operation 1: Write operation |

4.25. SATA1 PHY Configuration Register

This register is used to configure some control parameters of SATA1 PHY.

Address Offset: 0750-0753h

Attribute: R/W

Default value: FF9F_0403h

Size: 32 bits

Table 51. SATA1 PHY Configuration Register 1

| Bit Field | Name | Read/Write | Description |
|-----------|-------------|------------|---|
| 3 | Port_reset | R/W | Link Reset |
| 2 | PHY_reset | R/W | PHY Software Reset 0: Release reset 1: Hold reset |
| 1 | ref_use_pad | R/W | PHY Reference Clock Selection 0: Use internal reference clock 1: Use external reference clock |
| 0 | Reserved | R/W | Reserved |

Address Offset: 0754-0757h

Attribute: R/W

Default value: 7FFF_FFFFh

Size: 32 bits

Table 52. SATA1 PHY Configuration Register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---------------|
| 31 | Phy_power_down | R/W | PHY Powerdown |

4.26. SATA1 PHY Access Configuration Register

This group of registers is used to control the generation of configuration access operations to the SATA1 PHY internal control registers.

Address Offset: 0758-075Bh

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 53. SATA1 PHY Access Configuration Register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:16 | phy_cfg_data | R/W | PHY configuration reads and writes data. In the write operation, the data is written to this register first, and then the write operation is performed. In the read operation, the read data returned from PHY is stored into this register. |
| 15:0 | phy_cfg_addr | R/W | PHY Configuration Address |

Address Offset: 075C-075Fh

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 54. SATA1 PHY Access Configuration Register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|--|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|--|
| 2 | phy_cfg_done | R/W | The completion of one access to PHY indicates the completion of reading and writing to PHY. Write completion indicates that the written data has been written to the PHY internal register, and read completion indicates that the read data has been returned to the to the phy_cfg_data register |
| 1 | phy_cfg_disable | R/W | 0 - Reading or writing to this set of registers triggers a PHY configuration access operation 1 - Reading or writing to this set of registers does not trigger a PHY configuration access operation, but rather acts as a read or write operation to this register |
| 0 | phy_cfg_R/W | R/W | Start a read operation or a write operation. 0: Read operation 1: Write operation |

4.27. SATA2 PHY Configuration Register

This register is used to configure some control parameters of SATA2 PHY.

Address Offset: 0760-0763h

Attribute: R/W

Default value: FF9F_0403h

Size: 32 bits

Table 55. SATA2 PHY Configuration Register 1

| Bit Field | Name | Read/Write | Description |
|-----------|-------------|------------|---|
| 3 | Port_reset | R/W | Link Reset |
| 2 | PHY_reset | R/W | PHY Software Reset 0: Release reset 1: Hold reset |
| 1 | ref_use_pad | R/W | PHY Reference Clock Selection 0: Use internal reference clock 1: Use external reference clock |
| 0 | Reserved | R/W | Reserved |

Address Offset: 0764-0767h

Attribute: R/W

Default value: 7FFF_FFFFh

Size: 32 bits

Table 56. SATA2 PHY Configuration Register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---------------|
| 31 | Phy_power_down | R/W | PHY Powerdown |

4.28. SATA2 PHY Access Configuration Register

This group of registers is used to control the generation of configuration access operations to the SATA2 PHY internal control registers.

Address Offset: 0768-076Bh

Attribute: R/W

Default value: 0000_0000h

Size: 32 bits

Table 57. SATA2 PHY Access Configuration Register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:16 | phy_cfg_data | R/W | PHY configuration reads and writes data. In the write operation, the data is written to this register first, and then the write operation is performed. In the read operation, the read data returned from PHY is stored into this register. |
| 15:0 | phy_cfg_addr | R/W | PHY Configuration Address |

Address Offset: 076C-076Fh

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 58. SATA2 PHY Access Configuration Register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|---|
| 31:7 | Reserved | R/W | Reserved |
| 6 | phy_cfg_reset | R/W | PHY Configuration Reset, High Active |
| 5:3 | phy_cfg_state | RO | PHY Configuration Status Machine Status Indication |
| 2 | phy_cfg_done | R/W | PHY One access completion indicates the completion of this read/write to the PHY. Write completion indicates that the write indicates that the read data has been written to the internal register of PHY, and the read completion indicates that the read data has been returned to the phy_cfg_data register. |

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 1 | phy_cfg_disable | R/W | <p>0: Reading or writing to this set of registers triggers the PHY configuration access operation</p> <p>1: Reading or writing to this set of registers does not trigger a PHY configuration access operation, but is performed as a read or write to this register. read or write to this register</p> |
| 0 | phy_cfg_R/W | R/W | <p>Start a read operation or a write operation.</p> <p>0: Read operation</p> <p>1: Write operation</p> |

4.29. Memory Capacity Configuration Register

This set of registers is used to configure the capacity of the video memory. This register represents the mask of the memory BAR register, 0 means the corresponding bit of the memory BAR register is writable, 1 means not writable. The number of 1's represents the memory capacity. The default memory capacity is 256MB.

Address Offset: 3838-383Bh

Attribute: R/W

Default value: 0FFF_FFFFh

Size: 32 bits

Table 59. Memory capacity configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|---|
| 31 : 0 | gmem_bar_mask | R/W | <p>The lower 32 bits of the memory BAR register mask.</p> <p>0: The corresponding bit of the memory BAR is writable</p> <p>1: The corresponding bit of the memory BAR is not writable</p> |

Address Offset: 383C-383Fh

Attribute: R/W,

Default value: 0000_0000h

Size: 32 bits

Table 60. Memory capacity configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------|------------|--|
| 31:0 | gmem_bar_mask | R/W | <p>The high 32 bits of the memory BAR register mask.</p> <p>0: The corresponding bit of the memory BAR is writable</p> <p>1: The corresponding bit of the memory BAR is not writable</p> |

4.30. Bridge Identity register

This register contains the identification ID and revision number of the bridge.

Address Offset: 3FF8-3FFBh

Attribute: R0

Default value: See the description in the table below

Size: 32 bits

Table 61. Bridge Identity register 3

| Bit Field | Name | Read/Write | Description |
|-----------|-------------|------------|-------------------------|
| 31:24 | fix_id | RO | Bridge fixed ID (0x7A). |
| 23:0 | variable_id | RO | Bridge Variable ID. |

Address Offset: 3FFC-3FFFh

Attribute: RO

Default value: See the description in the table below

Size: 32 bits

Table 62. Bridge Identity register 4

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|-------------------------------|
| 31:24 | revision_number | RO | Bridge piece revision number. |
| 23:0 | Reserved | RO | Reserved |

Chapter 5. Interrupt Controller

The bridge chip has an integrated advanced programmable interrupt controller. The internal interrupt controller supports up to 64 interrupt sources and two interrupt outputs.

The bridge supports interrupt transmission via both interrupt lines and HT messages.

In the interrupt line method, the bridge's interrupt output pins are connected to the processor's interrupt input pins, and the processor is interrupted via the interrupt pins.

In the HT message method, no additional interrupt pin connection is required, and the bridge sends the interrupt vector to the processor's HT controller register by means of an HT packet, and the processor is interrupted by the HT controller interrupt.

The bridge chip supports the use of only one of these two interrupt methods and is valid for all 64 interrupt sources simultaneously.

The bridge supports outputting dual interrupts, meaning that interrupt information can be routed to both processors. The correspondence between interrupt sources and interrupt outputs is configurable, and this configuration is valid for both interrupt line and HT message packet interrupt modes.

In interrupt line interrupt mode, the interrupt lines of all interrupt-capable devices inside the bridge chip are sent directly to the bridge chip's interrupt controller, and external PCIE devices send interrupts to the bridge chip's internal PCIE controller via legacy interrupts. The bridge's interrupt controller finally interrupts the processor via the bridge's interrupt pin signal.

In HT message interrupt mode, all devices inside the bridge except the PCIE send interrupt information to the interrupt controller of the bridge via the interrupt line, and the interrupt controller converts the interrupt information into HT message packets and sends them to the processor via the HT bus.

For PCIE devices, there are two interrupt modes, one is that the device still uses legacy interrupt and sends the interrupt information to the interrupt controller of the bridge through the interrupt line of the PCIE controller of the bridge, and the interrupt controller is responsible for converting the interrupt information into HT message packets; the other is to enable the MSI interrupt function of the PCIE device, and the MSI interrupt message of the device passes through the PCIE controller of the bridge. The other is to enable the MSI interrupt function of the PCIE device, and the device's MSI interrupt messages are converted into HT packets by the conversion module inside the bridge's PCIE controller.

Note that in the latter mode, the interrupt packets of the PCIE device do not support interrupt routing and can only be sent to the HT Io controller of the bridge.

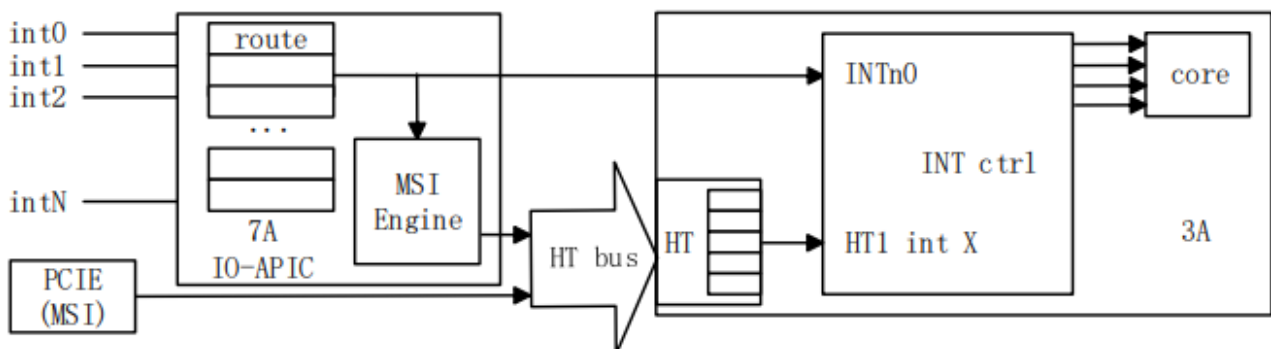


Figure 7. Schematic of the interrupt system of 3A + 7A

The figure above illustrates the hardware modules and processes involved in interrupts using the 3A+7A computer system as an example.

The figure shows the process of the two interrupt methods, the upper part shows the interrupt through the

interrupt line INTn0, and the lower part shows the interrupt through the HT message packet.

The interrupt intX from the device (except for PCIE devices operating in **MSI** mode) is sent to the 7A internal interrupt controller, where it is routed to the bridge pin or converted into an HT packet and sent to the 3A's HT controller, which receives the interrupt through the external interrupt pin or HT controller interrupt, and is routed through the interrupt to The interrupt controller of 3A receives the interrupt through external interrupt pin or HT controller interrupt and interrupts a processor core through interrupt route.

The address space of the bridge interrupt controller is 4KB, and the starting address (internal space of the bridge) is configured by the BIOS.

5.1. Interrupt Source Assignment

The internal devices of the bridge chip are connected to the interrupt controller via interrupt lines. The interrupt pin assignment of the interrupt controller is shown in the follow Table. AC97 controller and HDA controller share one interrupt pin, **GPI00-3** share one interrupt pin, and other **GPI0s** share one interrupt pin.

Table 63. Bridge chip interrupt controller interrupt source assignment

| Interrupt Pins | Interrupt Source | Interrupt Pins | Interrupt Source |
|----------------|------------------|----------------|------------------|
| 0 | - | 32 | pcie_f0_0 |
| 1 | - | 33 | pcie_f0_1 |
| 2 | - | 34 | pcie_f0_2 |
| 3 | - | 35 | pcie_f0_3 |
| 4 | - | 36 | pcie_f1_0 |
| 5 | - | 37 | pcie_f1_1 |
| 6 | - | 38 | pcie_h_lo |
| 7 | - | 39 | pcie_h_hi |
| 8 | uart[3:0] | 40 | pcie_g0_lo |
| 9 | i2c[5:0] | 41 | pcie_g0_hi |
| 10 | - | 42 | pcie_g1_lo |
| 11 | - | 43 | pcie_g1_hi |
| 12 | gmac0_sbd | 44 | toy[0] |
| 13 | gmac0_pmt | 45 | toy[1] |
| 14 | gmac1_sbd | 46 | toy[2] |
| 15 | gmac1_pmt | 47 | acpi_int |
| 16 | sata[0] | 48 | usb_0_ehci |
| 17 | sata[1] | 49 | usb_0_ohci |
| 18 | sata[2] | 50 | usb_1_ehci |
| 19 | lpc | 51 | usb_1_ohci |
| 20 | - | 52 | rtc[0] |
| 21 | - | 53 | rtc[1] |

| Interrupt Pins | Interrupt Source | Interrupt Pins | Interrupt Source |
|----------------|------------------|----------------|------------------|
| 22 | - | 54 | rtc[2] |
| 23 | - | 55 | hpet_int |
| 24 | pwm[0] | 56 | ac97_dma[0] |
| 25 | pwm[1] | 57 | ac97_dma[1] |
| 26 | pwm[2] | 58 | ac97/hda |
| 27 | pwm[3] | 59 | gpio_hi |
| 28 | dc | 60 | gpio[0] |
| 29 | gpu | 61 | gpio[1] |
| 30 | gmem | 62 | gpio[2] |
| 31 | thsens | 63 | gpio[3] |

5.2. Description of Interrupt-related Registers

The bridge chip's interrupt controller has a set of control and status registers for each interrupt source.

Table 64. Interrupt control and status registers

| Register Name | Length | Read/Write | Description | Default Value |
|---------------|--------|------------|--|---------------|
| INT_MASK | 1 | R/W | Interrupt Mask Register. 0: Enable the interrupt. 1: Mask this interrupt. | 1 |
| HTMSI_EN | 1 | R/W | HT packet interrupt enable register. 0: Turn off the HT message packet mode. 1: Enable the HT message packet mode. | 0 |
| INTEDGE | 1 | R/W | Trigger mode setting register. 0: Level-triggered interrupt. 1: Edge-triggered interrupt. | 0 |
| INTCLR | 1 | WO | Edge-triggered interrupt clear register. Write 1 clears the interrupt, write 0 has no effect. | N/A |

| Register Name | Length | Read/Write | Description | Default Value |
|---------------|--------|------------|--|---------------|
| AUTO_CTRL0 | 1 | R/W | <p>Interrupt distribution mode control register (used in conjunction with AUTO_CTRL1).</p> <p>{AUTO_CTRL1, AUTO_CTRL0}.</p> <p>00b: fixed distribution mode.</p> <p>01b: rotating distribution mode.</p> <p>10b: idle distribution mode.</p> <p>11b: Busy distribution mode.</p> | 0 |
| AUTO_CTRL1 | 1 | R/W | <p>Interrupt distribution mode control register (used in conjunction with AUTO_CTRL0).</p> <p>{AUTO_CTRL1, AUTO_CTRL0}.</p> <p>00b: fixed distribution mode.</p> <p>01b: rotating distribution mode.</p> <p>10b: idle distribution mode.</p> <p>11b: Busy distribution mode.</p> | 0 |
| ROUTE_ENTRY | 8 | R/W | <p>Interrupt Routing Register.</p> <p>Used to configure which processor to route this interrupt to. This register is organized in the form of a bitmap.</p> <p>Bit0: Routed to INTn0/HT controller lo; bit1: Routed to INTn1/HT controller hi. bit7:2: Reserved.</p> | 01b |
| HTMSI_VECTOR | 8 | R/W | HT message packet interrupt vector register. | See below |
| INTISR_CHIP0 | 1 | RO | <p>Routing to the interrupt status (in service) register of INTn0.</p> <p>0: no interrupts.</p> <p>1: with interrupts.</p> | 0 |
| INTISR_CHIP1 | 1 | RO | <p>Routing to INTn1's interrupt status (in service) register.</p> <p>0: no interrupts.</p> <p>1: with interrupts.</p> | 0 |

| Register Name | Length | Read/Write | Description | Default Value |
|---------------|--------|------------|---|---------------|
| INTIRR | 1 | RO | Interrupt request register. 0: no interrupt request. 1: Interrupt request is available. | 0 |
| INTISR | 1 | RO | Interrupt status (in service) register. 0: no interrupt is being received. 1: There are interrupts being received. | 0 |
| INT_POLARITY | 1 | R/W | Interrupt level trigger polarity selection register. For the level trigger type. 0: High level trigger. 1: Low level trigger. | 0 |

The address distribution of the registers related to the interrupt controller is shown in the following table

Interrupt register address distribution

Table 65. Interrupt register address distribution

| Register Name | Address Offset | Read/Write | Description |
|----------------|----------------|------------|--|
| INT_ID | 0x000 | RO | Interrupt controller identification register |
| INT_MASK | 0x020 | R/W | Interrupt Mask Register |
| HTMSI_EN | 0x040 | R/W | HT message packet interrupt enable register |
| INTEDGE | 0x060 | R/W | Trigger mode setting register |
| INTCLR | 0x080 | WO | Edge-triggered interrupt clear register |
| AUTO_CTRL0 | 0x0c0 | R/W | Interrupt distribution mode control register 0 |
| AUTO_CTRL1 | 0x0e0 | R/W | Interrupt distribution mode control register 1 |
| ROUTE_ENTRY_0 | 0x100 | R/W | Interrupt routing register [7- 0] |
| ROUTE_ENTRY_8 | 0x108 | R/W | Interrupt routing register [15- 8] |
| ROUTE_ENTRY_16 | 0x110 | R/W | Interrupt Routing Register [23-16] |
| ROUTE_ENTRY_24 | 0x118 | R/W | Interrupt Routing Register [31-24] |
| ROUTE_ENTRY_32 | 0x120 | R/W | Interrupt routing register [39-32] |
| ROUTE_ENTRY_40 | 0x128 | R/W | Interrupt Routing Register [47-40] |
| ROUTE_ENTRY_48 | 0x130 | R/W | Interrupt Routing Register [55-48] |
| ROUTE_ENTRY_56 | 0x138 | R/W | Interrupt Routing Register [63-56] |
| HTMSI_VECTOR0 | 0x200 | R/W | HT Interrupt Vector Register [7- 0] |
| HTMSI_VECTOR8 | 0x208 | R/W | HT Interrupt Vector Register [15- 8] |

| Register Name | Address Offset | Read/Write | Description |
|----------------|----------------|------------|--|
| HTMSI_VECTOR16 | 0x210 | R/W | HT Interrupt Vector Register [23-16] |
| HTMSI_VECTOR24 | 0x218 | R/W | HT Interrupt Vector Register [31-24] |
| HTMSI_VECTOR32 | 0x220 | R/W | HT Interrupt Vector Register [39-32] |
| HTMSI_VECTOR40 | 0x228 | R/W | HT Interrupt Vector Register [47-40] |
| HTMSI_VECTOR48 | 0x230 | R/W | HT Interrupt Vector Register [55-48] |
| HTMSI_VECTOR56 | 0x238 | R/W | HT Interrupt Vector Register [63-56] |
| INTISR_0 | 0x300 | RO | Interrupt status (in service) register routed to INTn0 |
| INTISR_1 | 0x320 | RO | Interrupt status (in service) register routed to INTn1 |
| INTIRR | 0x380 | RO | Interrupt request register |
| INTISR | 0x3a0 | RO | Interrupt Status (In Service) Register |
| INT_POLARITY | 0x3e0 | R/W | Interrupt trigger level selection register |

Interrupt controller identification register

Address Offset: 000-003h

Attribute: RO

Default value: 07000000h Size: 32 bits

Table 66. Interrupt controller identification register 1

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------------------|
| 31:24 | id | RO | Interrupt Controller ID |
| 23:0 | Reserved | RO | Reserved |

Address Offset: 004-007h

Attribute: RO

Default value: 003F0001h

Size: 32 bits

Table 67. Interrupt controller identification register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|--|
| 31:24 | Reserved | RO | Reserved |
| 23:16 | int_num | RO | The number of interrupt sources supported. The actual number of interrupts is equal to the value of this field plus 1. |
| 15:8 | Reserved | RO | Reserved |

| Bit Field | Name | Read/Write | Description |
|-----------|---------|------------|-------------------------------------|
| 7:0 | version | RO | Interrupt controller version number |

Interrupt mask register

Address Offset: 020-023h

Attribute: R/W

Default value: FFFFFFFFh

Size: 32 bits

Table 68. Interrupt mask register 1

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|--|
| 31:0 | int_mask | R/W | Low 32 bits of the interrupt mask register (bit[31:0]) |

Address Offset: 024-027h

Default value: FFFFFFFFh

Attribute: R/W

Size: 32 bits

Table 69. Interrupt mask register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|--|
| 31:0 | int_mask | R/W | High 32 bits of the interrupt mask register (bit[63:32]) |

HT interrupt message packet enable register

Address Offset: 040-043h

Default value: 00000000h

Attribute: R/W

Size: 32 bits

Table 70. HT interrupt message packet enable register 1

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|--|
| 31:0 | htmsi_en | R/W | Low 32 bits (bit[31:0]) of the HT Interrupt Message Packet Enable Register |

Address Offset: 044-047h

Default value: 00000000h

Attribute: R/W

Size: 32 bits

Table 71. HT interrupt message packet enable register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|--|
| 31:0 | htmsi_en | R/W | High 32 bits (bit[63:32]) of the HT Interrupt Message Packet Enable Register |

Interrupt trigger control register

Address Offset: 060-063h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 72. Interrupt trigger control register 1

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---|
| 31:0 | int_edge | R/W | Low 32 bits of the interrupt trigger control register (bit[31:0]) |

Address Offset: 064-067h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 73. Interrupt trigger control register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---|
| 31:0 | int_edge | R/W | High 32 bits of the interrupt trigger control register (bit[63:32]) |

Interrupt clear register

Address Offset: 080-083h

Attribute: WO

Default value: N/A

Size: 32 bits

Table 74. Interrupt clear register 1

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---|
| 31:0 | int_clear | WO | Low 32 bits of the interrupt clear register (bit`[31:0]`) |

Address Offset: 084-087h

Attribute: WO

Default value: 00000000h

Size: 32 bits

Table 75. Interrupt clear register 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---|
| 31:0 | int_clear | WO | High 32 bits of the interrupt clear register (bit[63:32]) |

INT_AUTO_CTRL0 register

Address Offset: 0C0-0C3h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 76. INT_AUTO_CTRL0 register 1

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|--|
| 31:0 | int_auto_ctrl0 | R/W | Low 32 bits (bit[31:0]) of Interrupt Smart Distribution Control Register 0 |

Address Offset: 0C4-0C7h

Default value: 00000000h

Attribute: R/W

Size: 32 bits

Table 77. INT_AUTO_CTRL0 register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|--|
| 31:0 | int_auto_ctrl0 | R/W | High 32 bits (bit[63:32]) of Interrupt Smart Distribution Control Register 0 |

INT_AUTO_CTRL1 register

Address Offset: 0E0-0E3h

Default value: 00000000h

Attribute: R/W

Size: 32 bits

Table 78. INT_AUTO_CTRL1 register 1

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|--|
| 31:0 | int_auto_ctrl1 | R/W | Low 32 bits (bit[31:0]) of Interrupt Smart Distribution Control Register 1 |

Address Offset: 0E4-0E7h

Default value: 00000000h

Attribute: R/W

Size: 32 bits

Table 79. INT_AUTO_CTRL1 register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 31:0 | int_auto_ctrl1 | R/W | High 32 bits (bit[63:32]) of Interrupt Smart Distribution Control Register `1 |

Interrupt routing configuration register

Address Offset: 100-103h

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 80. Interrupt routing configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 31:0 | Reserved | R/W | Reserved |

Address Offset: 104-107h

Default value: 01010101h

Attribute: R/W

Size: 32 bits

Table 81. Interrupt routing configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 31:0 | Reserved | R/W | Reserved |

Address Offset: 108-10Bh

Default value: 01010101h

Attribute: R/W

Size: 32 bits

Table 82. Interrupt routing configuration register 3

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 31:16 | Reserved | R/W | Reserved |
| 9:8 | i2c_int_route | R/W | I2C Interrupt Routing Configuration Register |
| 1:0 | uart_int_route | R/W | UART Interrupt Routing Configuration Register |

Address Offset: 10C-10Fh

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 83. Interrupt routing configuration register 4

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 25:24 | gmac1_pmt_int_route | R/W | GMAC1_PMT Interrupt Routing Configuration Register |
| 17:16 | gmac1_sbd_int_route | R/W | GMAC1_SBD Interrupt Routing Configuration Register |
| 9:8 | gmac0_pmt_int_route | R/W | GMAC0_PMT Interrupt Routing Configuration Register |
| 1:0 | gmac0_sbd_int_route | R/W | GMAC0_SBD Interrupt Routing Configuration Register |

Address Offset: 110-113h

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 84. Interrupt routing configuration register 5

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|--|
| 25:24 | lpc_int_route | R/W | LPC Interrupt Routing Configuration Register |
| 17:16 | SATA2_int_route | R/W | SATA2 Interrupt Routing Configuration Register |
| 9:8 | SATA1_int_route | R/W | SATA1 Interrupt Routing Configuration Register |
| 1:0 | SATA0_int_route | R/W | SATA0 Interrupt Routing Configuration Register |

Address Offset: 114-117h

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 85. Interrupt routing configuration register 6

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 31:0 | Reserved | R/W | Reserved |

Address Offset: 118-11Bh

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 86. Interrupt routing configuration register 7

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 25:24 | pwm3_int_route | R/W | PWM3 Interrupt Routing Configuration Register |
| 17:16 | pwm2_int_route | R/W | PWM2 Interrupt Routing Configuration Register |
| 9:8 | pwm1_int_route | R/W | PWM1 Interrupt Routing Configuration Register |
| 1:0 | pwm0_int_route | R/W | PWM0 Interrupt Routing Configuration Register |

Address Offset: 11C-11Fh

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 87. Interrupt routing configuration register 8

| Bit Field | Name | Read/Write | Description |
|-----------|------------------|------------|---|
| 25:24 | thsens_int_route | R/W | Thsensor Interrupt Routing Configuration Register |
| 17:16 | gpu_int_route | R/W | GPU Interrupt Routing Configuration Register |
| 9:8 | gmem_int_route | R/W | GMEM Interrupt Routing Configuration Register |
| 1:0 | dc_int_route | R/W | DC Interrupt Routing Configuration Register |

Address Offset: 120-123h

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 88. Interrupt routing configuration register 9

| Bit Field | Name | Read/Write | Description |
|-----------|----------------------|------------|---|
| 25:24 | pcie_f0_p3_int_route | R/W | PCIE_F0 Controller 3 Interrupt Routing Configuration Register |
| 17:16 | pcie_f0_p2_int_route | R/W | PCIE_F0 Controller 2 Interrupt Routing Configuration Register |
| 9:8 | pcie_f0_p1_int_route | R/W | PCIE_F0 Controller 1 Interrupt Routing Configuration Register |
| 1:0 | pcie_f0_p0_int_route | R/W | PCIE_F0 Controller 0 Interrupt Routing Configuration Register |

Address Offset: 124-127h

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 89. Interrupt routing configuration register 10

| Bit Field | Name | Read/Write | Description |
|-----------|----------------------|------------|---|
| 25:24 | pcie_h_p1_int_route | R/W | PCIE_H Controller 1 Interrupt Routing Configuration Register |
| 17:16 | pcie_h_p0_int_route | R/W | PCIE_H Controller 0 Interrupt Routing Configuration Register |
| 9:8 | pcie_f1_p1_int_route | R/W | PCIE_F1 Controller 1 Interrupt Routing Configuration Register |
| 1:0 | pcie_f1_p0_int_route | R/W | PCIE_F1 Controller 0 Interrupt Routing Configuration Register |

Address Offset: 128-12Bh

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 90. Interrupt routing configuration register 11

| Bit Field | Name | Read/Write | Description |
|-----------|----------------------|------------|---|
| 25:24 | pcie_g1_p1_int_route | R/W | PCIE_G1 Controller 1 Interrupt Routing Configuration Register |
| 17:16 | pcie_g1_p0_int_route | R/W | PCIE_G1 Controller 0 Interrupt Routing Configuration Register |
| 9:8 | pcie_g0_p1_int_route | R/W | PCIE_G0 Controller 1 Interrupt Routing Configuration Register |
| 1:0 | pcie_g0_p0_int_route | R/W | PCIE_G0 Controller 0 Interrupt Routing Configuration Register |

Address Offset: 12C-12Fh

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 91. Interrupt routing configuration register 12

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 25:24 | acpi_int_route | R/W | ACPI Interrupt Routing Configuration Register |

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 17:16 | toy2_int_route | R/W | TOY2 Interrupt Routing Configuration Register |
| 9:8 | toy1_int_route | R/W | TOY1 Interrupt Routing Configuration Register |
| 1:0 | toy0_int_route | R/W | TOY0 Interrupt Routing Configuration Register |

Address Offset: 130-133h

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 92. Interrupt routing configuration register 13

| Bit Field | Name | Read/Write | Description |
|-----------|------------------------|------------|---|
| 25:24 | usb1_ohci_int_route | R/W | USB1 OHCI Controller Interrupt Routing Configuration Register |
| 17:16 | usb1_ehci_p2_int_route | R/W | USB1 EHCI Controller Interrupt Routing Configuration Register |
| 9:8 | usb0_ohci_int_route | R/W | USB0 OHCI Controller Interrupt Routing Configuration Register |
| 1:0 | usb0_ehci_int_route | R/W | USB0 EHCI Controller Interrupt Routing Configuration Register |

Address Offset: 134-137h

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 93. Interrupt routing configuration register 14

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 25:24 | hpet_int_route | R/W | HPET Interrupt Routing Configuration Register |
| 17:16 | rtc2_int_route | R/W | RTC2 Interrupt Routing Configuration Register |
| 9:8 | rtc1_int_route | R/W | RTC1 Interrupt Routing Configuration Register |
| 1:0 | rtc0_int_route | R/W | RTC0 Interrupt Routing Configuration Register |

Address Offset: 138-13Bh

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 94. Interrupt routing configuration register 15

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 25:24 | gpio_hi_int_route | R/W | GPIO high bit (bit[56:4]) interrupt routing configuration register |
| 17:16 | ac97/hda_int_route | R/W | AC97/HDA controller interrupt routing configuration register |
| 9:8 | ac97_dma1_int_route | R/W | AC97 DMA1 Interrupt Routing Configuration Register |
| 1:0 | ac97_dma0_int_route | R/W | AC97 DMA0 Interrupt Routing Configuration Register |

Address Offset: 13C-13Fh

Attribute: R/W

Default value: 01010101h

Size: 32 bits

Table 95. Interrupt routing configuration register 16

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 25:24 | gpio3_int_route | R/W | GPIO3 Interrupt Routing Configuration Register |
| 17:16 | gpio2_int_route | R/W | GPIO2 Interrupt Routing Configuration Register |
| 9:8 | gpio1_int_route | R/W | GPIO1 Interrupt Routing Configuration Register |
| 1:0 | gpio0_int_route | R/W | GPIO0 Interrupt Routing Configuration Register |

HT message packet interrupt vector configuration register

Address Offset: 200-203h

Attribute: R/W

Default value: 03020100h

Size: 32 bits

Table 96. HT message packet interrupt vector configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 31:0 | Reserved | R/W | Reserved |

Address Offset: 204-207h

Attribute: R/W

Default value: 070605040h

Size: 32 bits

Table 97. HT message packet interrupt vector configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 31:0 | Reserved | R/W | Reserved |

Address Offset: 208-20Bh

Attribute: R/W

Default value: 0B0A0908h

Size: 32 bits

Table 98. HT message packet interrupt vector configuration register 3

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 31:16 | Reserved | R/W | Reserved |
| 15:8 | i2c_int_route | R/W | I2C HT Interrupt Vector Configuration Register |
| 7:0 | uart_int_route | R/W | UART HT interrupt vector configuration register |

Address Offset: 20C-20Fh

Attribute: R/W

Default value: 0E0F0D0Ch

Size: 32 bits

Table 99. HT message packet interrupt vector configuration register 4

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 31:24 | gmac1_pmt_int_route | R/W | GMAC1_PMT HT Interrupt Vector Configuration Register |
| 23:16 | gmac1_sbd_int_route | R/W | GMAC1_SBD HT Interrupt Vector Configuration Register |
| 15:8 | gmac0_pmt_int_route | R/W | GMAC0_PMT HT Interrupt Vector Configuration Register |
| 7:0 | gmac0_sbd_int_route | R/W | GMAC0_SBD HT Interrupt Vector Configuration Register |

Address Offset: 210-213h

Attribute: R/W

Default value: 13121110h

Size: 32 bits

Table 100. HT message packet interrupt vector configuration register 5

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|--|
| 31:24 | lpc_int_route | R/W | LPC HT Interrupt Vector Configuration Register |
| 23:16 | SATA2_int_route | R/W | SATA2 HT Interrupt Vector Configuration Register |
| 15:8 | SATA1_int_route | R/W | SATA1 HT Interrupt Vector Configuration Register |
| 7:0 | SATA0_int_route | R/W | SATA0 HT Interrupt Vector Configuration Register |

Address Offset: 214-217h

Attribute: R/W

Default value: 17161514h

Size: 32 bits

Table 101. HT message packet interrupt vector configuration register 6

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 31:0 | Reserved | R/W | Reserved |

Address Offset: 218-21Bh

Attribute: R/W

Default value: 1B1A1918h

Size: 32 bits

Table 102. HT message packet interrupt vector configuration register 7

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 31:24 | pwm3_int_route | R/W | PWM3 HT Interrupt Vector Configuration Register |
| 23:16 | pwm2_int_route | R/W | PWM2 HT Interrupt Vector Configuration Register |
| 15:8 | pwm1_int_route | R/W | PWM1 HT Interrupt Vector Configuration Register |
| 7:0 | pwm0_int_route | R/W | PWM0 HT Interrupt Vector Configuration Register |

Address Offset: 21C-21Fh

Attribute: R/W

Default value: 1E1F1D1Ch

Size: 32 bits

Table 103. HT message packet interrupt vector configuration register 8

| Bit Field | Name | Read/Write | Description |
|-----------|------------------|------------|---|
| 31:24 | thsens_int_route | R/W | Thsensor HT Interrupt Vector Configuration Register |
| 23:16 | gpu_int_route | R/W | GPU HT Interrupt Vector Configuration Register |
| 15:8 | gmem_int_route | R/W | GMEM HT Interrupt Vector Configuration Register |
| 7:0 | dc_int_route | R/W | DC HT Interrupt Vector Configuration Register |

Address Offset: 220-223h

Attribute: R/W

Default value: 43424140h

Size: 32 bits

Table 104. HT message packet interrupt vector configuration register 9

| Bit Field | Name | Read/Write | Description |
|-----------|----------------------|------------|---|
| 31:24 | pcie_f0_p3_int_route | R/W | PCIE_F0 Controller 3 HT Interrupt Vector Configuration Register |
| 23:16 | pcie_f0_p2_int_route | R/W | PCIE_F0 Controller 2 HT Interrupt Vector Configuration Register |
| 15:8 | pcie_f0_p1_int_route | R/W | PCIE_F0 Controller 1 HT Interrupt Vector Configuration Register |
| 7:0 | pcie_f0_p0_int_route | R/W | PCIE_F0 Controller 0 HT Interrupt Vector Configuration Register |

Address Offset: 224-227h

Attribute: R/W

Default value: 47464544h

Size: 32 bits

Table 105. HT message packet interrupt vector configuration register 10

| Bit Field | Name | Read/Write | Description |
|-----------|----------------------|------------|---|
| 31:24 | pcie_h_p1_int_route | R/W | PCIE_H Controller 1 HT Interrupt Vector Configuration Register |
| 23:16 | pcie_h_p0_int_route | R/W | PCIE_H Controller 0 HT Interrupt Vector Configuration Register |
| 15:8 | pcie_f1_p1_int_route | R/W | PCIE_F1 Controller 1 HT Interrupt Vector Configuration Register |
| 7:0 | pcie_f1_p0_int_route | R/W | PCIE_F1 Controller 0 HT Interrupt Vector Configuration Register |

Address Offset: 228-22Bh

Attribute: R/W

Default value: 4B4A4948h

Size: 32 bits

Table 106. HT message packet interrupt vector configuration register 11

| Bit Field | Name | Read/Write | Description |
|-----------|----------------------|------------|---|
| 31:24 | pcie_g1_p1_int_route | R/W | PCIE_G1 Controller 1 HT Interrupt Vector Configuration Register |
| 23:16 | pcie_g1_p0_int_route | R/W | PCIE_G1 Controller 0 HT Interrupt Vector Configuration Register |
| 15:8 | pcie_g0_p1_int_route | R/W | PCIE_G0 Controller 1 HT Interrupt Vector Configuration Register |

| Bit Field | Name | Read/Write | Description |
|-----------|----------------------|------------|---|
| 7:0 | pcie_g0_p0_int_route | R/W | PCIE_G0 Controller 0 HT Interrupt Vector Configuration Register |

Address Offset: 22C-22Fh

Attribute: R/W

Default value: 4F4E4D4Ch

Size: 32 bits

Table 107. HT message packet interrupt vector configuration register 12

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 31:24 | acpi_int_route | R/W | ACPI HT Interrupt Vector Configuration Register |
| 23:16 | toy2_int_route | R/W | TOY2 HT Interrupt Vector Configuration Register |
| 15:8 | toy1_int_route | R/W | TOY1 HT Interrupt Vector Configuration Register |
| 7:0 | toy0_int_route | R/W | TOY0 HT Interrupt vector configuration register |

Address Offset: 230-233h

Attribute: R/W

Default value: 53525150h

Size: 32 bits

Table 108. HT message packet interrupt vector configuration register 13

| Bit Field | Name | Read/Write | Description |
|-----------|------------------------|------------|---|
| 31:24 | usb1_ohci_int_route | R/W | USB1 OHCI Controller HT Interrupt Vector Configuration Register |
| 23:16 | usb1_ehci_p2_int_route | R/W | USB1 EHCI Controller HT Interrupt Vector Configuration Register |
| 15:8 | usb0_ohci_int_route | R/W | USB0 OHCI Controller HT Interrupt Vector Configuration Register |
| 7:0 | usb0_ehci_int_route | R/W | USB0 EHCI Controller HT Interrupt Vector Configuration Register |

Address Offset: 234-237h

Attribute: R/W

Default value: 57565554h

Size: 32 bits

Table 109. HT message packet interrupt vector configuration register 14

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|---|
| 31:24 | hpet_int_route | R/W | HPET HT Interrupt Vector Configuration Register |
| 23:16 | rtc2_int_route | R/W | RTC2 HT Interrupt Vector Configuration Register |
| 15:8 | rtc1_int_route | R/W | RTC1 HT Interrupt Vector Configuration Register |
| 7:0 | rtc0_int_route | R/W | RTC0 HT Interrupt Vector Configuration Register |

Address Offset: 238-23Bh

Attribute: R/W

Default value: 5B5A5958h

Size: 32 bits

Table 110. HT message packet interrupt vector configuration register 15

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 31:24 | gpio_hi_int_route | R/W | GPIO high bit (bit[56:4]) HT interrupt vector configuration register |
| 23:16 | ac97/hda_int_route | R/W | AC97/HDA Controller HT Interrupt Vector Configuration Register |
| 15:8 | ac97_dma1_int_route | R/W | AC97 DMA1 HT Interrupt vector configuration register |
| 7:0 | ac97_dma0_int_route | R/W | AC97 DMA0 HT Interrupt vector configuration register |

Address Offset: 23C-23Fh

Attribute: R/W

Default value: 5F5E5D5Ch

Size: 32 bits

Table 111. HT message packet interrupt vector configuration register 16

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|--|
| 31:24 | gpio3_int_route | R/W | GPI03 HT Interrupt Vector Configuration Register |
| 23:16 | gpio2_int_route | R/W | GPI02 HT Interrupt Vector Configuration Register |
| 15:8 | gpio1_int_route | R/W | GPI01 HT Interrupt Vector Configuration Register |
| 7:0 | gpio0_int_route | R/W | GPI00 HT Interrupt Vector Configuration Register |

Interrupts routed to INTn0 are in the Service Status Register

Address Offset: 300-303h

Attribute: R0

Default value: 00000000h

Size: 32 bits

Table 112. HT message packet interrupt vector configuration register 17

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---|
| 31:0 | int_isr_0 | R/W | Interrupts routed to INTn0 are in the lower 32 bits of the Service Status Register (bit [31:0]) |

Address Offset: 304-307h

Attribute: R0

Default value: 00000000h

Size: 32 bits

Table 113. HT message packet interrupt vector configuration register 18

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---|
| 31:0 | int_isr_0 | R/W | The interrupt routed to INTn0 is in the high 32 bits of the service status register (bit [63:32]) |

Interrupts routed to INTn1 are in the service status segiste

Address Offset: 320-323h

Attribute: R0

Default value: 00000000h

Size: 32 bits

Table 114. Interrupts routed to INTn1 are in the service status segister 1

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---|
| 31:0 | int_isr_1 | R/W | Interrupts routed to INTn1 are in the lower 32 bits of the service status register (bit [31:0]) |

Address Offset: 324-327h

Attribute: R0

Default value: 00000000h

Size: 32 bits

Table 115. Interrupts routed to INTn1 are in the service status segister 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---|
| 31:0 | int_isr_1 | R/W | The interrupt routed to INTn1 is in the high 32 bits of the service status register (bit [63:32]) |

Interrupt request register

Address Offset: 380-383h

Attribute: R0

Default value: 00000000h

Size: 32 bits

Table 116. Interrupt request register 1

| Bit Field | Name | Read/Write | Description |
|-----------|---------|------------|---|
| 31:0 | int_irr | R/W | Low 32 bits of the interrupt request register (bit`[31:0]`) |

Address Offset: 384-387h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 117. Interrupt request register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------|------------|---|
| 31:0 | int_irr | R/W | High 32 bits of the interrupt request register (bit`[63:32]`) |

Interrupt in service status register

Address Offset: 3A0-3A3h

Attribute: R0

Default value: 00000000h

Size: 32 bits

Table 118. Interrupt in service status register 1

| Bit Field | Name | Read/Write | Description |
|-----------|---------|------------|---|
| 31:0 | int_isr | R/W | Interrupt in the lower 32 bits of the service status register (bit`[31:0]`) |

Address Offset: 3A4-3A7h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 119. Interrupt in service status register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------|------------|---|
| 31:0 | int_isr | R/W | Interrupt in the high 32 bits of the service status register (bit`[63:32]`) |

Interrupt level trigger polarity register

Address Offset: 3E0-3E3h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 120. Interrupt level trigger polarity register 1

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 31:0 | int_polarity | R/W | Low 32 bits of the interrupt level trigger polarity register (bit `[31:0]`) |

Address Offset: 3E4-3E7h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 121. Interrupt level trigger polarity register 2

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 31:0 | int_polarity | R/W | High 32 bits of the interrupt level trigger polarity register (bit `[63:32]`) |

5.3. Device Interrupt Types

For the bridge chip, AC97 DMA interrupts are edge triggered, gpio interrupts can be configured to be level triggered or edge triggered as needed, and the rest of the interrupts are level triggered and active high.

For PCIE devices, one way is to use the interrupt line of the PCIE controller inside the bridge to transmit the interrupt; the other way is to use the MSI interrupt of the PCIE device directly.

In the PCIE MSI interrupt method, when the PCIE controller inside the bridge receives an MSI interrupt, it converts it directly into an HT interrupt message packet to send to the HT controller. Therefore, the software needs to be careful to distinguish the MSI interrupt vector of the PCIE device from the HT interrupt vector configured by the internal device of the bridge.

5.4. Interrupt Distribution Modes

The bridge supports dual interrupt outputs, so that different interrupt sources or multiple interrupts from the same interrupt source can be distributed between the two interrupt outputs. The bridge chip supports interrupt hardware load balancing, which allows interrupts to be distributed between the two outputs preset by software in four modes.:

1. Fixed distribution mode - Distribution is done according to the routing method configured in the interrupt routing configuration register. In this mode, the routing configuration register must be one-hot encoded, meaning that an interrupt can only be routed to one interrupt output.
2. Rotating distribution mode - In this mode, each new interrupt generated is routed to the next valid interrupt output according to the route vector configuration in the Route_Entry register. The route to the next valid interrupt output is configured in the Route_Entry register.

3. Idle distribution mode - jumps to an idle interrupt output. In this mode, when each new interrupt is generated, it first detects if there is already an unprocessed interrupt on the next interrupt output according to the routing vector configuration in the Entry register, and if not, it is routed to that interrupt output; if there is already an unprocessed interrupt on the next interrupt output, it continues to detect the next processor core.
4. Busy distribution mode - the current interrupt output is busy then jumps to its left (0→1→2→3) candidate interrupt output. When each new interrupt is generated in this mode, it first detects whether there is already an unprocessed interrupt on the interrupt output of the last interrupt, and if not, continues to interrupt that interrupt output, and if there is an unprocessed interrupt, it is routed to the next interrupt output as configured in the Entry register. It should be noted that once AUTO_CTRL0/1 has been configured, it should not be modified in the middle of the run. It is recommended that the software use fixed distribution mode.

5.5. Detailed Description of Interrupt Handling Process

In the interrupt line interrupt mode, the interrupt controller of the bridge chip receives the device interrupt and sets the corresponding interrupt output pin low according to the interrupt routing configuration. The processor receives the interrupt through the interrupt input pin, and the processor obtains the current interrupt source routed to itself by reading the corresponding ISR (interrupt in service register) register within the bridge chip interrupt controller. The interrupt processing process is:

1. The interrupt controller of the bridge receives the device interrupt; (hardware)
2. The interrupt controller of the bridge chip sets the interrupt output pin low; (hardware)
3. The processor's interrupt controller receives the interrupt pin interrupt; (hardware)
4. The processor turns off the interrupt. (software)
5. The processor reads its own interrupt controller and learns that it is an external interrupt; (software)
6. The processor reads the interrupt controller of the bridge chip to get the interrupt vector; (software)
7. The processor writes the interrupt controller of the bridge chip to mask the corresponding interrupt source; (software)
8. The processor opens the interrupt. (software)
9. The processor calls the interrupt service program to handle the interrupt; (software)
10. The processor writes the bridge chip's interrupt controller to clear edge-triggered interrupts; (software)
11. The processor writes the bridge chip's interrupt controller to turn on the corresponding interrupt source. (Software)
12. The processor interrupt returns. (Software)

In the HT message packet interrupt method, the interrupt controller and PCIE controller of the bridge receive the device interrupt and can send the interrupt vector directly to the HT controller of the processor, thus avoiding the process of the processor querying the internal interrupt vector of the bridge. The interrupt processing process is as follows.

1. The interrupt controller of the bridge receives the device interrupt; (hardware)
2. The interrupt controller of the bridge slices sends the interrupt vector to the HT controller of the processor; (hardware)
3. The processor's interrupt controller receives the HT interrupt; (hardware)
4. The processor turns off the interrupt. (software) 5.
5. The processor reads its own interrupt controller and learns that it is an HT interrupt; (software)
6. The processor reads its own HT controller to get the interrupt vector; (software)
7. The processor writes its own HT controller to clear the interrupt; (software)
8. The processor opens the interrupt. (software) 9.

9. The processor calls the interrupt service program to handle the interrupt; (software)
10. The processor writes the bridge chip's interrupt controller to clear the interrupt (not required if it is an MSI interrupt issued by a PCIE device). (software)
11. The processor interrupt returns. (Software)

The software can configure the HT interrupt vector corresponding to the internal devices of the bridge chip.

Chapter 6. HPET Controller

The HPET controller is compatible with standard specifications. Internally, it includes a 64-bit main counter and three 32-bit timers (comparators). Of the three timers, timer 0 supports both periodic-capable and non-periodic interrupts, while timers 1 and 2 support only non-periodic interrupts.

6.1. Access Address

The address space size of the HPET controller is 4KB, and the starting address (internal space of the bridge chip) is configured by the BIOS. The physical address composition of the internal registers of the HPET controller is as follows:

Table 122. Access address

| Address bits | Composition | Remarks |
|--------------|-------------|---------------------------|
| [11:08] | 0 | Reserved |
| [07:00] | REG | Internal register address |

Note: The HPET controller only supports 4-byte accesses. Software that needs to use the HPET's 64-bit master counter as a timestamp needs to be careful to handle the data rounding introduced by reading the high and low 32-bit values in two separate readings.

6.2. Description of Registers

Table 123. HPET register list

| Register Offset Address | Description |
|-------------------------|---|
| 000-007h | General Capabilities and ID Register |
| 008-00Fh | Reserved |
| 010-017h | General Configuration Register |
| 018-01Fh | Reserved |
| 020-027h | General Interrupt Status Register |
| 028-0EFh | Reserved |
| 0F0-0F7h | Main Counter Value Register |
| 100-107h | Timer 0 Configuration and Capability Register |
| 108-10Fh | Timer 0 Comparator Value Register |
| 110-11Fh | Reserved |
| 120-127h | Timer 1 Configuration and Capability Register |
| 128-12Fh | Timer 1 Comparator Value Register |
| 130-13Fh | Reserved |
| 140-147h | Timer 2 Configuration and Capability Register |
| 148-14Fh | Timer 2 Comparator Value Register |
| 150-15Fh | Reserved |

General Capabilities and ID Register

Address Offset: 00-07h

Attribute: RO

Default value: See description

Size: 8

Table 124. General capabilities and id register

| Bit Field | Name | Description | Read/Write |
|-----------|--------------------|---|------------|
| 63:32 | COUNTER_CLK_PERIOD | Timing frequency of the master timer in fps (10^{15} s). Default value: 1312D00h (20ns clock period). | RO |
| 31:16 | VENDOR_ID | Manufacturer ID. value: 0014h | RO |
| 15:14 | Reserved | Reserved | RO |
| 13 | COUNT_SIZE_CAP | The width of the master timer. This chip is a 64-bit master timer. Value: 1b. 0: 32 bits 1: 64 bits | RO |
| 12:8 | NUM_TIM_CAP | Number of timers; the value of this field indicates the number of the last timer. This chip contains 3 timers. This chip contains 3 timers. Value: 2h. | RO |
| 7:0 | REV_ID | Version number; value: 02h | RO |

General Configuration Register

Address Offset: 10-17h

Attribute: RO, R/W

Default value: 0h

Size: 8

Table 125. General configuration register

| Bit Field | Name | Description | Read/Write |
|-----------|------------|---|------------|
| 63:1 | Reserved | Reserved | RO |
| 0 | ENABLE_CNF | HPET enable control. 0: the main timer stops timing and all timers are no longer generating interrupts. 1: the main timer counts and the timers are allowed to generate interrupts. | |

General Interrupt Status Register

Address Offset: 20-27h

Attribute: RO, R/WC

Default value: 0h

Size:8

Table 126. General interrupt status register

| Bit Field | Name | Description | Read/Write |
|-----------|------------|--|------------|
| 63 : 3 | Reserved | Reserved | RO |
| 2 | T2_INT_STS | Timer 2 interrupt status. Same function as T0_INT_STS. | R/WC |
| 1 | T1_INT_STS | Timer 1 interrupt status. Same function as T0_INT_STS. | R/WC |
| 0 | T0_INT_STS | Timer 0 interrupt state. When the timer's interrupt trigger mode is level-triggered, this timer defaults to 0. When the corresponding timer interrupt occurs, then the hardware will set it to 1. Once set, software writing 1 to this timer will clear it. Once it is set, software writing 1 to this timer will clear this timer. Writing 0 to this timer will be meaningless. When the interrupt triggering mode of the timer is edge triggering mode. Software will ignore this bit. Software usually writes 0 to this bit. | R/WC |

The interrupt trigger mode of each timer is determined by the Tn_TYPE_CNF bit of the respective Configuration and Capability register.

Main Counter Value Register

Address Offset: F0-F7h

Attribute: R/W

Default value: 0h

Size: 8

Table 127. Main counter value register

| Bit Field | Name | Description | Read/Write |
|-----------|--------------|--|------------|
| 63 : 0 | Main_Counter | Master timer. Modifying the value of this register is only allowed when the main timer stops timing. | R/W |

Timer 0 Configuration and Capabilities Register

Address Offset: 100-107h

Attribute: RO, R/W

Default value: 10h

Size: 8

Table 128. Timer 0 configuration and capabilities register

| Bit Field | Name | Description | Read/Write |
|-----------|---------------------|---|------------|
| 63:9 | Reserved | Reserved | RO |
| 8 | T0_32MODE_CN F | Timer 0 32-bit mode configuration. When the timer is 64-bit, the software writes 1 to this bit to use the timer as a 32-bit. This version of the timer does not support 64-bit, and the bit is not writable. | RO |
| 7 | Reserved | Reserved | RO |
| 6 | T0_VAL_SET_CN NF | Timer 0 value setting. Only timers that can generate periodic interrupts will use this field. By writing 1 to this field, software can directly modify the periodic. The software can directly modify the accumulator for the periodic period by writing 1 to this field. Software does not need to clear 0 to this field. | R/W |
| 5 | T0_SIZE_CAP | Timer 0 Width indication. 0: 32-bit width 1: 64-bit width | RO |
| 4 | T0_PER_INT_CN AP | Timer 0 Periodic interrupt indication. 1: the timer is capable of generating periodic interrupts. 0: the timer is not capable of generating periodic interrupts. | RO |
| 3 | T0_TYPE_CNF | Timer 0 cycle interrupt configuration. If the corresponding T0_PER_INT_CAP bit is 0, then this bit is read-only and defaults to 0. If the corresponding T0_PER_INT_CAP bit is 1, then this bit is readable and writable. It is used to enable the corresponding timer to generate periodic interrupts. 1: Enable the timer to generate periodic interrupts 0: Enable the timer to generate non-periodic interrupts | R/W |
| 2 | T0_INT_ENB_CN NF | Enable Timer 0 to generate interrupts | R/W |
| 1 | T0_INT_TYPE_CN F | Timer 0 interrupt type configuration. 0: The interrupt triggering mode of the timer is edge triggered; this means that the corresponding timer will generate an edge triggered interrupt. If another interrupt is generated, then another edge will be generated. 1: The interrupt trigger mode of the timer is level triggered; this means that the corresponding timer will generate a level triggered interrupt. This interrupt will remain active until it is cleared by software (General Interrupt Status Register). | R/W |

| Bit Field | Name | Description | Read/Write |
|-----------|----------|-------------|------------|
| 0 | Reserved | Reserved | RO |

Timer 0 Comparator Value Register

Address Offset: 108-10Fh

Attribute: R/W

Default value: FFFFFFFFh

Size: 8

Table 129. Timer 0 comparator value register

| Bit Field | Name | Description | Read/Write |
|-----------|------------|---|------------|
| 63:32 | Reserved | Reserved | RO |
| 31:0 | T0_Com_VAL | The value of the timer 0 comparator. When the corresponding timer is configured in non-periodic mode, the value of this register will be compared with the value of the main timer register. If the value of the main timer is equal to the value of the comparator, a timing interrupt is generated (if; the corresponding interrupt enable is on). The comparator value will not change due to the interrupt generation. If the corresponding timer is configured in periodic mode, interrupt is generated when the value of the comparator in the value field of the main timer is equal (if; the corresponding interrupt enable is turned on). If an interrupt is generated, then the comparator value is accumulated from the last software write to the comparator. For example, when the comparator value is written to 0x0123h then an interrupt is generated when the value of the main timer is 0x123h; the comparator value is modified by hardware to 0x246h. When the value of the main timer reaches 0x246h, another interrupt is generated; the comparator value is modified by hardware to 0x369h. Whenever an interrupt is generated, the comparator value will be accumulated; until the comparator value reaches the maximum (0xffffffff), then the accumulator value will continue to accumulate. For example, when the comparator value is FFFF0000h, and the last time the comparator was written by software, the value is 20000. When the interrupt occurs, the comparator value becomes 00010000h. | R/W |

Timer 1 Configuration and Capabilities Register

Address Offset: 120-127h

Attribute: RO, R/W

Default value: 00h

Size: 8 Timer 1 configuration and function registers. Same as Timer 0.

Timer 1 Comparator Value Register

Address Offset: 128-12Fh

Attribute: R/W

Default value: FFFFFFFFh

Size: 8 Timer 1 comparator value. Same as Timer 0.

Timer 2 Configuration and Capabilities Register

Address Offset: 140-147h

Attribute: RO, R/W

Default value: 00h

Size: 8

Timer 2 configuration and function registers. Same as Timer 0.

Timer 2 Comparator Value Register

Address Offset: 148-14Fh

Attribute: R/W

Default value: FFFFFFFFh

Size: 8

Timer 2 comparator value. Same as Timer 0.

Chapter 7. HT Controller

The bridge HT interface supports a maximum bi-directional 16-bit data width and an operating frequency of 2.0 GHz. After the connection is established by automatic system initialization, the user can change the width and operating frequency and re-initialize by modifying the corresponding configuration registers in the protocol.

The main features of the bridge HT interface are as follows:

- Support HT1.0/3.0 protocol
- Support 200/400/800/1600/2000 MHz operating frequency
- Support 8/16 bit width
- Support dual processors with bridge chip direct connection (each link can only work in 8-bit mode)

7.1. HT User Guide

7.1.1. HT Working Mode

When chip pin HT_8x2 is configured to 0, the bridge operates in single mode, where only one processor is directly connected to the bridge via the HT bus, and only one HT controller (HT lo) is operating inside the bridge, while the other HT controller (HT hi) is not available.

The HT link can operate in either 8-bit or 16-bit mode, and the software can configure the data width used (the maximum available width also depends on the PCB hardware connection), when the data link is controlled by controller lo. The data link is controlled by the controller lo.

When the chip pin HT_8x2 is configured to 1, the bridge operates in dual mode, where two processors can be connected directly to the bridge via the HT bus, and the two HT controllers inside the bridge are operating simultaneously, controlling the low 8 bits and high 8 bits of the data link respectively. Software can control both HT controllers via the HT bus of both processors. When operating in dual mode, the software needs to configure the HT DMA routing configuration (see section 4.1 HT Clock Enable and DMA Routing Configuration) to send DMA accesses to the corresponding HT controller.

7.1.2. HT Address Space

The address space for processor accesses is described in Section 3.

The HT module has several internal address windows for configuring CPU accesses and DMA accesses. For CPU accesses, the bridge chip acts as the accessee and the corresponding configuration window is called the receive window; for DMA accesses, the bridge chip acts as the access initiator and the corresponding window is called the send window.

The receive window consists of two types: the P2P access window and the normal access window. Accesses that fall within the P2P access window are forwarded directly back to the HT bus as P2P commands and are not sent to the internal devices of the bridge chip; accesses that fall within the normal access window are sent to the internal devices of the bridge chip as accesses to the internal devices of the bridge chip. The P2P access window has a higher priority than the normal access window. Accesses that do not hit in either of the two types of receive windows are forwarded directly back to the HT bus as P2P commands.

DMA accesses are sent out through the HT's non-Post channel by default, and the Post send window is set internally in the bridge to send DMA accesses out through the HT's Post channel. That is, DMA accesses that hit in the Post send window are sent to the HT bus via the HT's Post channel, and DMA accesses that do not hit in the Post send window are sent to the HT bus via the HT's non-Post channel. In general, the Post send window should not be enabled and all DMA accesses should be sent out through the HT's non-Post channel.

7.2. HT Configuration Register

HT Configuration Register

Table 130. HT configuration register

| Address Offset | Abbreviations | Description | Default value | Read/Write |
|----------------|---------------|--|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A00h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 06h-07h | PCISTS | PCI Status | 0010h | RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 00h | RO |
| 0Bh | BCC | Base Class Code | 06h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 80h | RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0014h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 7A00h | RO |
| 34h | CAPP | Capabilities Pointer | 40h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 00h | RO |
| 3Eh-3Fh | BCTRL | Bridge Control Register | 0000h | R/W |
| 42h-43h | DIDCMD | Device ID Command Register | 0000h | R/W, RO |
| 44h-45h | LKSC0 | Link Status and Control Register 0 | 0020h | R/W |
| 46h-47h | LKWDSC0 | Link Width Status and Control Register 0 | 0000h | R/W |
| 4Ch | HTRID | HT Revision ID | 60h | RO |
| 4Dh-4Fh | LKFREQSC0 | Link Frequency Status and Control Register 0 | 000000h | R/W, RO |
| 140h-147h | RXWIN0 | Receive Window 0 | 0000F00080000000h | R/W |
| 148h-14Fh | RXWIN1 | Receive Window 1 | FDFCFFFF80000000h | R/W |
| 150h-157h | RXWIN2 | Receive Window 2 | 0000000000000000h | R/W |
| 158h-15Fh | RXWIN3 | Receive Window 3 | 0000000000000000h | R/W |
| 160h-167h | RXWIN4 | Receive Window 4 | 0000000000000000h | R/W |
| 170h-177h | TXPOSTWIN0 | Transmit Post Window 0 | 0000000000000000h | R/W,RO |
| 178h-17Fh | TXPOSTWIN1 | Transmit Post Window 1 | 0000000000000000h | R/W,RO |
| 1B0h-1B7h | RXP2PWIN0 | Receive P2P Window 0 | 0000000000000000h | R/W,RO |

| Address Offset | Abbreviations | Description | Default value | Read/Write |
|----------------|---------------|-------------------------|-------------------|------------|
| 1B8h-1BFh | RXP2PWIN1 | Receive P2P Window 1 | 0000000000000000h | R/W,RO |
| 1F4h-1F7h | HTPLLCTRL | HT PII Control Register | 00000000h | R/W,RO |

Note: Address spaces not listed in the table indicate reservations.

BCTRL-HT bridge control register

Address Offset: 3E-3Fh

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 131. BCTRL-HT bridge control register

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---|
| 15:7 | Reserved | RO | Reserved |
| 6 | HT Reset | R/W | This bit controls the HT reset. 0: unreset. 1: Reset. |
| 5:0 | Reserved | RO | Reserved |

DIDCMD - device ID command register

Address Offset: 42-43h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 132. DIDCMD-device ID command register

| Bit Field | Name | Read/Write | Description |
|-----------|----------------|------------|--|
| 15:13 | Command Format | RO | Command Format |
| 12:10 | Reserved | RO | Reserved |
| 9:5 | Unit Count | R/W | Provided to the software for recording the current number of units |
| 4:0 | Unit ID | R/W | Record the number of IDs used |

LKSC0-Link status control register 0

Address Offset: 44-45h

Attribute: R/W, RO

Default value: 2000h

Size: 16 bits

Table 133. LKSC0-Link status control register 0

| Bit Field | Name | Read/Write | Description |
|-----------|--------------------------|------------|---|
| 15:14 | Reserved | RO | Reserved |
| 13 | LDTSTOP# Tristate Enable | R/W | Whether to turn off the HT PHY when the HT bus enters the HT Disconnect state. 0: Not to turn off; 1: To turn off. |
| 12:10 | Reserved | RO | Reserved |
| 9 | CRC Error (hi) | R/W | CRC error occurs in high 8 bits |
| 8 | CRC Error (lo) | R/W | CRC error occurs on low 8 bits |
| 7 | Trans off | R/W | HT PHY off control. When in 16-bit bus operation, 1: Turn off the high/low 8-bit HT PHY; 0: Enable the low 8-bit HT PHY, the high 8-bit HT PHY is controlled by bit 0 |
| 6 | End of Chain | RO | HT Bus End |
| 5 | Init Complete | RO | HT bus initialization complete |
| 4 | Link Fail | RO | Connection failure indication |
| 3:2 | Reserved | RO | Reserved |
| 1 | CRC Flood Enable | R/W | Whether to flood the HT bus in case of CRC error |
| 0 | Trans off (hi) | R/W | When running an 8-bit protocol using a 16-bit HT bus, the high 8-bit PHY is off control. 0: Enables the high 8-bit HT PHY. 1: Disables high 8-bit HT PHY. |

LKWDSC0-Link data width status and control register

Address Offset: 46-47h

Attribute: R/W, RO

Default value: 0011h or 0000h

Table 134. LKWDSC0-Link data width status and control register

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 15 | Reserved | RO | Reserved |

| Bit Field | Name | Read/Write | Description |
|-----------|-------------------|------------|--|
| 14:12 | Link TX Width | R/W | <p>Link Sender Width. The value after a cold reset is the maximum width of the current connection, and the value written to this register will take effect after the next hot reset or HT Disconnect.</p> <p>000b: 8 bits.</p> <p>001b: 16 bits.</p> |
| 11 | Reserved | RO | Reserved |
| 10:8 | Link RX Width | R/W | <p>Link Sender Width. The value after a cold reset is the maximum width of the current connection, and the value written to this register will take effect after the next hot reset or HT Disconnect.</p> <p>000b: 8 bits.</p> <p>001b: 16 bits.</p> |
| 7 | TX DW FC | RO | <p>The transmitter supports double-word flow control.</p> <p>0: not supported.</p> <p>1: Supported.</p> |
| 6:4 | Link TX Max Width | RO | <p>Maximum width of the link transmitter.</p> <p>000b: 8 bits.</p> <p>001b: 16 bits.</p> |
| 3 | RX DW FC | RO | <p>The receiver side supports double-word flow control.</p> <p>0: Not supported.</p> <p>1: Supported.</p> |
| 2:0 | Link RX Max Width | RO | <p>Maximum width at the receiver end of the link.</p> <p>000b: 8 bits.</p> <p>001b: 16 bits.</p> <p>Note: When HT_8x2 is 0, the default value is 0011h; when HT_8x2 is 1, the default value is 0000h.</p> |

LKFREQCFG0-Link frequency configuration register

Address Offset: 4C-4Dh

Attribute: R/W, RO

Default value: 0060h

Size: 32 bits

Table 135. LKFREQCFG0-Link frequency configuration register 1

| Bit Field | Name | Read/Write | Description |
|-----------|------------------------|------------|---|
| 15:14 | Reserved | RO | Reserved |
| 13 | Overflow Error | RO | HT bus packet overflow |
| 12 | Protocol Error | RO | Protocol error, referring to an unrecognized command received on the HT bus |
| 11:8 | Link Frequency Control | R/W | HT Bus Operating Frequency Configuration, the configuration value corresponds to the bit of Link Frequency Capability. For example, setting this register to 4 means that the HT bus frequency is configured to 600 MHz (the frequency represented by bit 4 of Link Frequency Capability). The value written to this register must be the value available as indicated by the Link Frequency Capability register (corresponding to a bit equal to 1). Writing to this register will take effect after the next thermal reset or HT Disconnect (when using the software configuration) |
| :0 | Revision ID | RO | PLL (0x1F4), this bit has no meaning) |

Address Offset: 4E-4Fh

Attribute: RO

Default value: 0000h

Table 136. LKFREQCFG0-Link frequency configuration register 2

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------------|------------|---|
| 15:0 | Link Frequency Capability | RO | <p>The supported HT bus frequency, which produces a different value depending on the external PLL setting (when using the software configuration PLL (0x1F4) is used, this bit is meaningless). Each bit represents an HT bus frequency, and when the bit is 1 it indicates that the frequency is supported; when the bit is 0 it indicates that the frequency is not supported. The frequencies represented by each bit are as follows:</p> <p>bit0:200MHz bit1:300MHz bit2:400MHz bit3:500MHz bit4:600MHz bit5:800MHz bit6:1.0GHz bit7:1.2GHz bit8:1.4GHz bit9:1.6GHz bit10:1.8GHz bit11:2.0GHz bit12:2.2GHz bit13:2.4GHz bit14:2.6GHz bit15:3.2GHz</p> |

RXWIN - receive address window

Receive address window hits are sent to the internal devices of the bridge chip only when the access is hit. The receive address window includes the following fields:

Table 137. RXWIN-receive address window

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---------------------|
| 64:48 | WIN_BASE | R/W | Window Base Address |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 47:32 | WIN_MASK | R/W | Window Mask |
| 31 | WIN_EN | R/W | Window Enable |
| 30 | WIN_TRANS_EN | R/W | Window address conversion enable |
| 29:0 | WIN_TRANS | R/W | Window converted address high bit of address bit[53:24] When the window is enabled, the address window hit condition is: (ADDR & WIN_MASK) == (WIN_BASE & WIN_MASK). If address translation is enabled, the output address is: (ADDR & ~WIN_MASK) |

RXWIN0-Receive window register 0

Address Offset: 140-147h

Attribute: R/W

Default value: 0000F00080000000h

Size: 64 bit

Table 138. RXWIN0-Receive window register 0

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|--|
| 64:48 | RXWIN0_BASE | R/W | Receive Window 0 Base Address |
| 47:32 | RXWIN0_MASK | R/W | Receive Window 0 Mask |
| 31 | RXWIN0_EN | R/W | Receive Window 0 Enable |
| 30 | RXWIN0_TRANS_EN | R/W | Receive Window 0 Address Conversion Enable |
| 29:0 | RXWIN0_TRANS | R/W | Receive Window 0 Converted high address, bit[53:24] of address |

RXWIN1-Receive window register 1

Address Offset: 148-14Fh

Attribute: R/W

Default value: FDFCFFFF80000000h

Size: 64 bit

Table 139. RXWIN1-Receive window register 1

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|--|
| 64:48 | RXWIN1_BASE | R/W | Receive Window 1 Base Address |
| 47:32 | RXWIN1_MASK | R/W | Receive Window 1 Mask |
| 31 | RXWIN1_EN | R/W | Receive Window 1 Enable |
| 30 | RXWIN1_TRANS_EN | R/W | Receive Window 1 Address Conversion Enable |

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 29:0 | RXWIN1_TRANS | R/W | Receive Window 1 Converted high address, bit `[53:24]` of the address |

RXWIN2-Receive window register 2

Address Offset: 150-147h |Attribute: R/W Default value: 0000000000000000h |Size: 64 bit

Table 140. RXWIN2-Receive window register 2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 64:48 | RXWIN2_BASE | R/W | Receive Window 2 Base Address |
| 47:32 | RXWIN2_MASK | R/W | Receive Window 2 Mask |
| 31 | RXWIN2_EN | R/W | Receive Window 2 Enable |
| 30 | RXWIN2_TRANS_EN | R/W | Receive Window 2 Address Conversion Enable |
| 29:0 | RXWIN2_TRANS | R/W | Receive Window 2 Converted High Address, bit `[53:24]` of the address |

RXWIN3-Receive window register 3

Address Offset: 158-14Fh

Attribute: R/W

Default value: 0000000000000000h

Size: 64 bit

Table 141. RXWIN3-Receive window register 3

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------|------------|---|
| 64:48 | RXWIN3_BASE | R/W | Receive Window 3 Base Address |
| 47:32 | RXWIN3_MASK | R/W | Receive Window 3 Mask |
| 31 | RXWIN3_EN | R/W | Receive Window 3 Enable |
| 30 | RXWIN3_TRANS_EN | R/W | Receive Window 3 Address Conversion Enable |
| 29:0 | RXWIN3_TRANS | R/W | Receive Window 3 Converted High Address, bit `[53:24]` of the address |

RXWIN4-Receive window register 4

Address Offset: 160-147h

Attribute: R/W

Default value: 0000000000000000h

Size: 64 bit

Table 142. RXWIN4-Receive window register 4

| Bit Field | Name | Read/Wri te | Description |
|-----------|-----------------|----------------|---|
| 64:48 | RXWIN4_BASE | R/W | Receive Window 4 Base Address |
| 47:32 | RXWIN4_MASK | R/W | Receive Window 4 Mask |
| 31 | RXWIN4_EN | R/W | Receive Window 4 Enable |
| 30 | RXWIN4_TRANS_EN | R/W | Receive Window 4 Address Conversion Enable |
| 29:0 | RXWIN4_TRANS | R/W | Receive Window 4 Converted High Address, bit `[53:24]` of the address |

TXPOSTWIN - quick send window

Visits hit by the Quick Send window give a direct response, thus speeding up the request for the request initiator. The Quick Send window includes the following fields:

Table 143. TXPOSTWIN - quick send window

| Bit Field | Name | Read/Wri te | Description |
|-----------|----------|----------------|---------------------|
| 64:48 | WIN_BASE | R/W | Window Base Address |
| 47:32 | WIN_MASK | R/W | Window Mask |
| 31 | WIN_EN | R/W | Window Enable |
| 30:0 | Reserved | R0 | Reserved |

When the window is enabled, the address window hit condition is: $(ADDR \& WIN_MASK) == (WIN_BASE \& WIN_MASK)$. Note: ADDR here refers to the high 16 bits of the address (bit `[39:24]`, the address sent to the HT bus is only 40 bits). For example, `1111111100000000b, 1100000000000000b` are all legal configurations, while The number of zeros in MASK indicates the size of the address window.

TXPOSTWIN0-Quick send window register 0

Address Offset: 170-177h

Attribute: R/W, R0

Default value: 0000000000000000h

Size: 64 bit

Table 144. TXPOSTWIN0-Quick send window register 0

| Bit Field | Name | Read/Wri te | Description |
|-----------|-----------------|----------------|----------------------------------|
| 64:48 | TXPOSTWIN0_BASE | R/W | Quick Send Window 0 Base Address |
| 47:32 | TXPOSTWIN0_MASK | R/W | Fast Send Window 0 Mask |
| 31 | TXPOSTWIN0_EN | R/W | Fast Send Window 0 Enable |
| 30:0 | Reserved | R0 | Reserved |

TXPOSTWIN1 - Quick send window register 1

Address Offset: 178-17Fh

Attribute: R/W, R0

Default value: 000000000000000h

Size: 64 bit

Table 145. TXPOSTWIN1-Quick send window register 1

| Bit Field | Name | Read/Wri te | Description |
|-----------|-----------------|----------------|----------------------------------|
| 64:48 | TXPOSTWIN1_BASE | R/W | Quick Send Window 1 Base Address |
| 47:32 | TXPOSTWIN1_MASK | R/W | Fast Send Window 1 Mask |
| 31 | TXPOSTWIN1_EN | R/W | Fast Send Window 1 Enable |
| 30:0 | Reserved | R0 | Reserved |

RXP2PWIN-P2P receive window

Accesses hit by the P2P receive window are sent directly back to the HT bus as P2P commands. the P2P receive window has a higher priority than the normal receive window. the P2P receive window includes the following fields.

Table 146. RXP2PWIN-P2P receive window

| Bit Field | Name | Read/Wri te | Description |
|-----------|----------|----------------|---------------------|
| 64:48 | WIN_BASE | R/W | Window Base Address |
| 47:32 | WIN_MASK | R/W | Window Mask |
| 31 | WIN_EN | R/W | Window Enable |
| 30:0 | Reserved | R0 | Reserved |

When the window is enabled, the address window hit condition is: (ADDR & WIN_MASK) == (WIN_BASE & WIN_MASK). Note: ADDR here refers to the high 16 bits of the address (bit[39:24], the address sent to the HT bus is only 40 bits).

For example, 1111111100000000b,1100000000000000b are legal configurations, while 1011111100000000b,11010000000000b are not. The number of zeros in MASK indicates the size of the address window.

RXP2PWIN0-P2P receive window 0

Address Offset: 180-187h

Attribute: R/W, R0

Default value: 00000`000000000000h

Size: 64 bit

Table 147. RXP2PWIN0-P2P receive window 0

| Bit Field | Name | Read/Wri te | Description |
|-----------|----------------|----------------|-----------------------------------|
| 64:48 | RXP2PWIN0_BASE | R/W | P2P Receive Window 0 Base Address |
| 47:32 | RXP2PWIN0_MASK | R/W | P2P receive window 0 mask |
| 31 | RXP2PWIN0_EN | R/W | P2P receive window 0 enable |
| 30:0 | Reserved | R0 | Reserved |

RXP2PWIN0-P2P receive window 1

Address Offset: 188-18Fh

Attribute: R/W, R0

Default value: 000000000000000h

Size: 64 bit

Table 148. RXP2PWIN1-P2P receive window 1

| Bit Field | Name | Read/Wri te | Description |
|-----------|----------------|----------------|-----------------------------------|
| 64:48 | RXP2PWIN1_BASE | R/W | P2P Receive Window 1 Base Address |
| 47:32 | RXP2PWIN1_MASK | R/W | P2P receive window 1 mask |
| 31 | RXP2PWIN1_EN | R/W | P2P receive window 1 enable |
| 30:0 | Reserved | R0 | Reserved |

Htpllctrl-ht pll control register

This register is used to enable the software configuration of the HT's PLL, which is used to modify the frequency of the HT PHY and controller.

Address Offset: 1F4-1F7h

Attribute: R/W, R0

Default value: 00000000h

Size: 32 bits

Table 149. Htpllctrl-ht pll control register

| Bit Field | Name | Read/Wri te | Description |
|-----------|----------------|----------------|---------------------------------|
| 31:26 | Reserved | R/W | Reserved |
| 25:22 | pll_div_phy_lo | R/W | PHY low output crossover |
| 21:18 | pll_div_phy_hi | R/W | PHY high output crossover |
| 17:16 | pll_div_refc | R/W | HT PLL input frequency division |
| 15:9 | pll_loopc | R/W | HT PLL Multiplier |

| Bit Field | Name | Read/Write | Description |
|-----------|-------------------|------------|------------------------------|
| 8:5 | pll_div_ctrl | R/W | Controller output divider |
| 4 | Reserved | R0 | Reserved |
| 3 | pll locked | R0 | PLL lock |
| 2 | Controller bypass | R/W | Controller clock bypass mode |
| 1 | pll config enable | R/W | PLL Configuration Enable |
| 0 | Reserved | R0 | 0: Disable PLL configuration |

Chapter 8. MISC Low-speed Devices

MISC low speed devices include: UART, I2C, PWM, ACPI, RTC, and GPIO. these devices run at a fixed frequency of 50MHz.

8.1. MISC Low-speed Devices Configuration Register

The address space size of the MISC low-speed device block is 512KB, and the starting address (internal space of the bridge chip) is configured by the BIOS.

8.2. Internal Device Address Routing

Multiple devices within the MISC low-speed device block are distinguished by the bits [18:16] of the address bits, and different devices support only specific types of access. The device routing and supported access types are shown in the following table.

Table 150. MISC Low-speed device address routing and access types

| bit[18:16] | 0 | 1 | 2 | 5 | 6 |
|------------|------|-----|-----|----------|------|
| Device | UART | I2C | PWM | ACPI/RTC | GPIO |
| Read/Write | B | B | W | W | B |

For UART, I2C, PWM, and ACPI/RTC, they require further routing due to the inclusion of multiple controllers. The internal routing of these device blocks is shown in the flow table. The number of routing address bits required varies from one device block to another.

Table 151. MISC Low-speed device address routing

| | 0 | 1 | 2 | 3 | 4 | 5 |
|------------------|-------|-------|-------|-------|------|------|
| UART(bit[9:8]) | UART0 | UART1 | UART2 | UART3 | - | - |
| I2C(bit[10:8]) | I2C0 | I2C1 | I2C2 | I2C3 | I2C4 | I2C5 |
| PWM(bit[9:8]) | PWM0 | PWM1 | PWM2 | PWM3 | - | - |
| ACPI/RTC(bit[8]) | ACPI | RTC | - | - | - | - |

These low-speed devices are described separately in subsequent sections.

Chapter 9. UART Controller

The integrated UART controller of the bridge chip complies with the RS232 standard and the controller is designed to be compatible with the 16550A. The internal clock frequency of the UART controller is 50 MHz and the maximum baud rate supported by the UART bus is 460800.

The bridge chip integrates four UART controllers, which are arranged in the UART module. In addition, UART1, UART2 and UART3 can only work in two-wire UART mode, and UART0 can work in full-function UART mode or two-wire UART mode. In addition, UART can be multiplexed as GPIO function and some UART pins can be multiplexed as I2C function. The pin multiplexing configuration registers related to UART are described in Section 4.4.

Table 152. UART function reuse

| UART_TXD/RXD | UART_RTS/CTS | UART_DTR/DSR | UART_RI/DCD |
|--------------|--------------|--------------|-------------|
| UART0 | | | |
| UART0 | UART1 | UART2 | UART3 |

9.1. Access Address

The access base address of the UART controller is the base address of the MISC low-speed device block plus offset 0x0. Note: The UART module supports byte access only.

The 4 UART controllers are distinguished by bit [9:8], and the internal physical address division of the UART module is shown in the following table.

Table 153. Module physical address composition

| Address bit | Composition | Remarks |
|-------------|-------------|------------------------------------|
| [15:10] | 0 | Reserved |
| [09:08] | UART number | 0x0 - 0x3 for each UART controller |
| [07:00] | REG | internal register address |

9.2. Description of Registers

Data register (DAT)

Offset: 0x00

Reset value: 0x00

Table 154. UART function reuse

| Bit Field | Name | Length | Read/Write |
|-------------|------|---------|------------|
| Description | 7:0 | Tx FIFO | 8 |

Interrupt enable register (IER)

Offset: 0x01

Reset value: 0x00

Table 155. Interrupt enable register (IER)

| Bit Field | Name | Length | Read/Write | Description |
|-----------|----------|--------|------------|---|
| 7:4 | Reserved | 4 | R/W | Reserved |
| 3 | IME | 1 | R/W | Modem Status Interrupt Enable 0: off 1: On |
| 2 | ILE | 1 | R/W | Receiver line status interrupt enable 0: off 1: Open |
| 1 | ITxE | 1 | R/W | Transmission save register is air break enable 0: off 1: open |
| 0 | IRxE | 1 | R/W | Receive valid data interrupt enable 0: off 1: Open |

Interrupt identification register (IIR)

Offset: 0x02

Reset value: 0xc1

Table 156. Interrupt identification register (IIR)

| Bit Field | Name | Length | Read/Write | Description |
|-----------|----------|--------|------------|---|
| 7:4 | Reserved | 4 | R | Reserved |
| 3:1 | II | 3 | R | Interrupt source indication bits, see the following table for details |
| 0 | INTp | 1 | R | Interrupt bits |

Interrupt control menu

Table 157. Interrupt control menu

| Bit 3 | Bit 2 | Bit 1 | Priority | Interrupt Type | Interrupt Source | Interrupt Reset Control |
|-------|-------|-------|----------|---------------------|-----------------------------------|---|
| 0 | 1 | 1 | 1st | Receive line status | parity, overflow or frame errors. | Read LSR |
| 0 | 1 | 0 | 2nd | Valid data received | or interrupt interrupt | The number of characters in the FIFO is lower than the value of the trigger |

| Bit 3 | Bit 2 | Bit 1 | Priority | Interrupt Type | Interrupt Source | Interrupt Reset Control |
|-------|-------|-------|----------|-------------------------------------|---|--------------------------------|
| 1 | 1 | 0 | 2nd | Receive timeout | The number of characters in the FIFO reaches the level of a trigger | Read the receive FIFO |
| 0 | 0 | 1 | 3rd | Transmission save register is empty | There is at least one character in the FIFO, but no operation, including read and write operations, within 4 characters | Write data to THR or multi-IIR |
| 0 | 0 | 0 | 4th | Modem Status | Transfer save register is empty | Read MSR |

FIFO control register (FCR)

Offset: 0x02

Reset value: 0xc0

Table 158. FIFO control register (FCR)

| Bit Field | Name | Length | Read/Write | Description |
|-----------|----------|--------|------------|---|
| 7:6 | TL | 2 | W | Receive trigger value for interrupt request from FIFO 00b: 1 byte 01b: 4 bytes 10b: 8 bytes 11b: 14 bytes |
| 5:3 | Reserved | 3 | W | Reserved |
| 2 | Txset | 1 | W | Clears the contents of the transmit FIFO and resets its logic |
| 1 | Rxset | 1 | W | Clears the contents of the receive FIFO and resets its logic |
| 0 | Reserved | 1 | W | Reserved |

Line control register (LCR)

Offset: 0x03

Reset value: 0x03

Table 159. Line control register (LCR)

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------|--------|------------|---|
| 7 | dlab | 1 | R/W | Crossover latch access bits 1: Access to operate the divider latch. 0: Access to operate the normal register. |
| 6 | bcb | 1 | R/W | Interrupt control bit 1: The output of the serial port is set to 0 (interrupt state) at this time. 0: Normal operation. |
| 5 | spb | 1 | R/W | Specify the parity bit 0: No parity bit is specified. 1: If the LCR[4] bit is 1, the transmit and check parity bit is 0. If the LCR[4] bit is 0, the transmit and check parity bit is 1. If the LCR[4] bit is 0, then the transmit and check parity bit is 1. |
| 4 | eps | 1 | R/W | Parity Bit Selection 0: Odd number of 1's per character (including data and parity bits). 1: Even 1's in each character. |
| 3 | pe | 1 | R/W | Parity bit enable 0: No parity bit. 1: Parity bit is generated at output, and parity bit is judged at input. |
| 2 | sb | 1 | R/W | Define the number of bits to generate stop bits 0: 1 stop bit. 1: 1.5 stop bits at 5-bit character length, 2 stop bits at other lengths. |
| 1:0 | bec | 2 | R/W | Set the number of bits per character 00b: 5 bits. 01b: 6 bits. 10b: 7 bits. 11b: 8 bits. |

MODEM control register (MCR)

Offset: `0x04`

Reset value: `0x00`

Table 160. MODEM control register (MCR)

| Bit Field | Name | Length | Read/Write | Description |
|-----------|----------|--------|------------|---|
| 7:5 | Reserved | 3 | W | Reserved |
| 4 | Loop | 1 | W | Loopback mode control bits 0: Normal operation. 1: Loopback mode. In loopback mode, the TXD output is always 1 and the output shift register is connected directly to the input shift register. Other connections are as follows: DTR - DSR RTS - CTS Out1 - RI Out2 - DCD |
| 3 | OUT2 | 1 | W | Connects to the DCD input in loopback mode |
| 2 | OUT1 | 1 | W | Connects to the RI input in loopback mode |
| 1 | RTSC | 1 | W | RTS signal control bit |
| 0 | DTRC | 1 | W | DTR signal control bit |

Line status register (LSR)

Offset: `0x05`

Reset value: `0x00`

Table 161. Line status register (LSR)

| Bit Field | Name | Length | Read/Write | Description |
|-----------|-------|--------|------------|---|
| 7 | ERROR | 1 | R | Error indication bit 0: No errors. 1: At least one of parity bit error, frame error or interrupt interrupt. one. |
| 6 | TE | 1 | R | Transfer to empty indicates bit 0: Data is available. 1: Both the transmit FIFO and the transmit shift register are empty. Clear when writing data to the transfer FIFO is cleared when writing data to the FIFO. |
| 5 | TFE | 1 | R | Transfer FIFO bit null indicates bit 0: Data is available. 1: The current transmit FIFO is empty and is cleared when writing data to the transmit FIFO. |

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------|--------|------------|---|
| 4 | BI | 1 | R | Interrupt interrupt indication bit 0: No interrupt. 1: Received Start bit + data + parity bit + stop bit are 0, i.e., there is an interrupt interrupt . |
| 3 | FE | 1 | R | Frame error indication bits 0: There are no errors. 1: The received data has no stop bit. |
| 2 | PE | 1 | R | Parity bit error indication bit 0: There is no parity error. 1: There is a parity error in the current received data. |
| 1 | OE | 1 | R | Data overflow indication bit 0: No overflow. 1: There is data overflow. |
| 0 | DR | 1 | R | Receive data valid indication bit 0: No data in the FIFO. 1: There is data in the FIFO. |

When reading this register, LSR[4:1] and LSR[7] are cleared to zero, LSR[6:5] is cleared when writing data to the transmit FIFO, and LSR[0] is judged for the receive FIFO.

MODEM status register (MSR)

Offset: 0x06

Reset value: 0x00

Table 162. MODEM status register (MSR)

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------|--------|------------|---|
| 7 | CDCD | 1 | R | The inverse of the DCD input value, or to Out2 in loopback mode |
| 6 | CRI | 1 | R | The inverse of the RI input value, or to OUT1 in loopback mode |
| 5 | CDSR | 1 | R | The inverse of the DSR input value, or to DTR in loopback mode |
| 4 | CCTS | 1 | R | The inverse of the CTS input value, or to RTS in loopback mode |
| 3 | DDCD | 1 | R | DDCD indication bit |
| 2 | TERI | 1 | R | RI edge detection, RI state changes from low to high |
| 1 | DDSR | 1 | R | DDSR indication bit |

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------|--------|------------|---------------------|
| 0 | DCTS | 1 | R | DCTS indication bit |

Frequency divider latch

Offset: 0x00

Reset value: 0x00

Table 163. Frequency divider latch 1

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------|--------|------------|---|
| 7:0 | LSB | 8 | R/W | Store the lower 8 bits of the divider latch |

Offset:0x01

Reset value:0x00

Table 164. Frequency divider latch 2

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------|--------|------------|--|
| 7:0 | MSB | 8 | R/W | Store the high 8 bits of the divider latch |

The value of the crossover latch {MSB, LSB} is calculated as $50\text{MHz}/16/\text{baud rate}$. For example, if you want to configure a serial port baud rate of 115200, the value of the divider latch = $50,000,000/16/115,200 \approx 27$.

Chapter 10. I2C Controller

A total of 6 I2C controllers are integrated into the bridge, and the I2C controllers operate at **50MHz**. The maximum transfer rate supported by the I2C bus is **400kbps**.

10.1. Access Address and Pin Multiplexing

The base address of accessing the I2C controller is the base address of the MISC low-speed device block plus an offset of **0x10000**.

Note: The I2C module only supports access by 1 byte.

The physical address composition of the I2C module internal registers is as follows.

Table 165. The physical address composition of the I2C module internal registers

| Address bits | Composition | Note |
|--------------|-----------------------|--|
| [15:11] | 0 | Reserved |
| [10:8] | I2C controller number | 0x0-0x5 represent I2C0-I2C5 respectively |
| [7:3] | 0 | Reserved |
| [2:0] | REG | Internal registers address |

For I2C modules, the corresponding pins should be set to the corresponding functions when used. The pin settings related to I2C are described in [Pin Multiplexing Configuration Register](#).

10.2. Description of I2C Controller Register

Frequency Division Latch Low-order Byte Register (PRER1o)

Offset: **0x00**

Reset value: **0xff**

Table 166. Frequency division latch low-order byte register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|--------|--------|------------|--|
| 7:0 | PRER1o | 8 | R/W | Store the lower 8 bits of the division latch |

Frequency Division Latch High-order Byte Register (PRERhi)

Offset: **0x01**

Reset value: **0xff**

Table 167. Frequency division latch high-order byte register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|--------|--------|------------|---|
| 7:0 | PRERhi | 8 | RW | Store the high 8 bits of the division latch |

Assuming that the value of the divider latch is **Prescaler** and the frequency of the I2C controller is **50MHz**,

if the clock frequency of the I2C bus is needed `clock_s`, then `Prescaler` should be equal to:
 $50M/(5*clock_s) - 1$.

Control Register (CTR)

Offset: `0x02`

Reset value: `0x00`

Table 168. Control register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|----------|--------|------------|---|
| 7 | EN | 1 | R/W | Module enable bit 0: Module disable 1: Module enable |
| 6 | IEN | 1 | R/W | Interrupt enable bit 0: Interrupt disable 1: Interrupt enable |
| 5:0 | Reserved | 6 | R/W | Reserved |

Transport Data Register (TXR)

Offset: `0x03`

Reset value: `0x00`

Table 169. Transport data register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|----------------|--------|------------|---|
| 7:1 | DATA[7:1]/ADDR | 7 | W | When transporting data, the data to be sent (<code>bit[7:1]</code>) is stored. When transporting the address, the address of the I2C slave device is stored |
| 0 | DATA[0]/RW | 1 | W | When transporting data, stores the data to be sent (<code>bit[0]</code>). When transporting the address, the read and write status is stored. 0: Write 1: Read |

Receive Data Register (RXR)

Offset: `0x03`

Reset value: 0x00

Table 170. Receive data register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------|--------|------------|---------------------|
| 7:0 | RXR | 8 | R | Store received data |

Command Control Register (CR)

Offset: 0x04

Reset value: 0x00

Table 171. Command control register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|----------|--------|------------|--|
| 7 | STA | 1 | W | Generate the START signal |
| 6 | STO | 1 | W | Generate the STOP signal |
| 5 | RD | 1 | W | Generate the read signal |
| 4 | WR | 1 | W | Generate the write signal |
| 3 | ACK | 1 | W | Generate the response signal 0: The controller sends ack at the end of this transmission 1: The controller does not send ack at the end of this transmission |
| 2:1 | Reserved | 2 | W | Reserved |
| 0 | IACK | 1 | W | Generate interrupt response signal. Software writes 1 to this bit to clear the interrupt. |

State Register (SR)

Offset: 0x04

Reset value: 0x00

Table 172. State register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|-------|--------|------------|---|
| 7 | RxACK | 1 | R | Receive response bit 1 - no receive the response bit 0 - receive the response bit |
| 6 | Busy | 1 | R | I2c bus busy flag bit 1 - bus is busy 0 - bus is free |

| Bit Field | Name | Length | Read/Write | Description |
|-----------|----------|--------|------------|--|
| 5 | AL | 1 | R | When the I2C core loses control of the I2C bus, this bit is 1 |
| 4:2 | Reserved | 3 | R | Reserved |
| 1 | TIP | 1 | R | Indicate the process of transport 1 - indicate that data is being transported 0 - indicate that data transport is complete |
| 0 | IF | 1 | R | Interrupt flag bit. When one data transport is finished, or another device initiates data transport, this bit is 1 |

Chapter 11. PWM Controller

A four-way pulse width output/counter controller (PWM) is implemented in the bridge. The four PWMs work and control in exactly the same way. Each PWM pin can be used as either a pulse output signal or a pulse width measurement input signal. The PWM controller clock is 50MHz, and the count and reference registers are 32-bit length.

11.1. Access Address and Pin Multiplexing

The base address of accessing the PWM controller is the base address of the MISC low-speed device block plus an offset of 0x20000.

Note: The PWM module only supports access by 4 bytes.

The physical address composition of the PWM controller internal registers is as follows.

Table 173. The physical address composition of the PWM controller internal registers

| Address bits | Composition | Note |
|--------------|-------------|--|
| [15:10] | 0 | Reserved |
| [9:8] | PWM number | 0x0-0x3 represent PWM0-PWM3 respectively |
| [7:4] | 0 | Reserved |
| [3:0] | REG | Internal registers address |

For PMM modules, the corresponding pins should be set to the corresponding functions when used. The pin settings related to PMM are described in [Pin Multiplexing Configuration Register](#).

11.2. Description of Registers

There are three registers per controller, which are described as follows.

Table 174. List of PWM registers

| Name | Address | Length | Read/Write | Description |
|-------------|------------|--------|------------|-----------------------------|
| low_buffer | Base + 0x4 | 32 | R/W | Low pulse width register |
| full_buffer | Base + 0x8 | 32 | R/W | Pulse period width register |
| CTRL | Base + 0xC | 11 | R/W | Control register |

PWM Control Register Configuration

| Bit Field | Name | Read/Write | Reset Value | Description |
|-----------|----------|------------|-------------|---|
| 0 | EN | R/W | 0 | PWM enable bit 1: PWM enable 0: PWM disable |
| 2:1 | Reserved | R/W | 0 | Reserved |

| Bit Field | Name | Read/Write | Reset Value | Description |
|-----------|--------|------------|-------------|--|
| 3 | OE | R/W | 0 | <p>Pin pulse output enable control bit (active low). When set to 1, the PWM can be used as a periodic interrupt generation module without changing the value of the PWM pin (held at 0)</p> <p>0: Pulse output enable</p> <p>1: Pulse output disable</p> |
| 4 | SINGLE | R/W | 0 | <p>Single pulse control bit, valid for non-measurement mode</p> <p>1: Pulse is generated only once</p> <p>0: Pulse is generated continuously</p> |
| 5 | INTE | R/W | 0 | <p>Interrupt enable bit. In the non-measurement mode, an interrupt is generated for every pulse period measured. In the measurement mode, an interrupt is generated when the input pulse period is greater than 0xFFFF_FFF9.</p> <p>1: Interrupt is generated</p> <p>0: No interrupt is generated</p> |
| 6 | INT | R/W | 0 | <p>Interrupt status bit. Write 1 to this bit to clear the interrupt</p> <p>1: The interrupt is generated</p> <p>0: No interrupt</p> |
| 7 | RST | R/W | 0 | <p>Counter reset</p> <p>1: Reset</p> <p>0: Normal work</p> |
| 8 | CAPTE | R/W | 0 | <p>Measurement pulse enable</p> <p>1: Measurement pulse mode</p> <p>0: Non-measurement pulse mode (or pulse output mode in general)</p> |

| Bit Field | Name | Read/Write | Reset Value | Description |
|-----------|--------|------------|-------------|--|
| 9 | INVERT | R/W | 0 | Output invert enable, valid for non-measurement mode 1: Invert the signal after the pulse is output (period starts at high level) 0: Keeps the pulse at the original output (period starts at low level) |
| 10 | DZONE | R/W | 0 | Anti dead zones function enable, valid for non-measurement mode 1: This PWM enables the anti dead zones function 0: This PWM disables the anti dead zones function |

11.3. Description of Functions

11.3.1. Pulse Width Modulation Function

The `low_buffer` and `full_buffer` registers are used to configure the low level of the periodic signal and the length of the total period of the PWM output in the clock period of the PWM module (20ns), respectively. For example, to generate a low pulse width of 50 times the PWM module clock period and a high pulse width of 90 times the PWM module clock period, you should configure the value 50 in the `low_buffer` and $(50+90)=140$ in the `full_buffer`.

The pulse width register value should be written before the `CTRL` control register. Before writing a new number to the pulse width register, you should clear the `EN` bit in the control register and then set the `EN` bit to 1 after writing the new number.

If 0 is written to both buffer registers, the output is always low. If writing 0 to `low_buffer` and 1 to `full_buffer`, the output is always high. If the value written to `low_buffer` is not less than the value of `full_buffer`, the output is low.

11.3.2. Pulse Measurement Function

After setting the `CTRL` control register, the PWM continuously samples the input signal level. When a down-jump of the input pulse signal is detected, the internal counter starts counting from 1, and when an up-jump is detected, the counter value is shifted to the `low_buffer` register and continues to accumulate, and when a down-jump is detected again, the counter value is shifted to the `full_buffer` register. For example, if the input pulse is 50 times the low pulse width of the system clock and 90 times the high pulse width, the final value read in the `low_buffer` is 50, and the value read in the `full_buffer` register is $(50+90)=140$.

It should be noted that the pulse to be measured should be a periodic signal, and the pulse period should not exceed the range that the 32-bit counter can measure. If there is a pulse with a pulse period longer than `0xFFFF_FFF9`, the `INT` bit of the control register will be set to 1, indicating that the pulse to be measured is out of the measurement range.

11.3.3. Anti Dead Zones Function

Multiple PWMs are equipped with an anti dead zones function between them, which prevents multiple pulse outputs from jumping at the same time. To use the anti dead zones function, the multiple PWMs of the anti dead zones function must be numbered from 0 and be consecutive, and their anti dead zones functions must all be enabled. In other words, one of PWM0/1, PWM0/1/2 and PWM0/1/2/3 must be used when using the anti dead zones function.

For PWM_0, PWM_1, PWM_2, and PWM_3, their priority is $0 > 1 > 2 > 3$. If they jump at the same time, PWM_1 will jump only after PWM_0 jumps (the lower priority signal is “erased” by one clock cycle), and so on. This priority is fixed and cannot be changed.

A typical anti dead zones example is as follows (PWM_* is the output when the anti dead zones function is disabled, and PWM_*' is the output when the anti dead zones function is enabled).

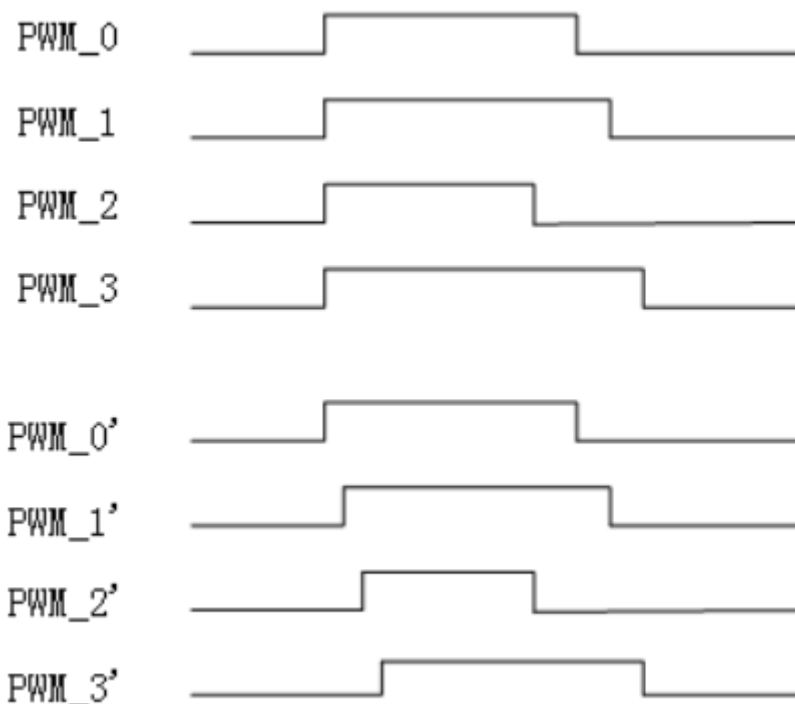


Figure 8. Anti dead zones function

Chapter 12. Power Management Module (ACPI Support)

Bridge power management module provides system power management functions. It supports **Advanced Configuration and Power Interface, Version 4.0a (ACPI)** to provide the corresponding power management functions.

- System hibernation and wake-up, support for ACPI S3 (suspend to RAM), ACPI S4 (suspend to disk), ACPI S5 (soft off), and support for power failure detection and automatic system recovery. It also supports multiple wake-up methods (USB, GMAC, power switch, etc.)
- System clock control, module clock gating, multiple ways to adjust the frequency.
- It integrates a watchdog with a maximum timing time of about **82s**.

12.1. Access Address

The base address of accessing the power management module is the base address of the MISC low-speed device block plus an offset of **0x50000**.

Note: The PWM module only supports access by 4 bytes.

The physical address composition of the ACPI module internal registers is as follows.

Table 175. The physical address composition of the ACPI controller internal registers

| Address bits | Composition | Note |
|--------------|-------------|----------------------------|
| [15:8] | 0 | Reserved |
| [7:0] | REG | Internal registers address |

12.2. Power Level

Table 176. Description of ACPI status

| | |
|-------|---|
| G0/S0 | Work all. The system works all in this mode |
| G1/S1 | Not supported at the moment |
| G1/S3 | Suspend to RAM (STR). Context saving to memory |
| G1/S4 | Suspend to Disk (STD). Save to hard disk, except wake-up circuit all power down |
| G2/S5 | Soft off. Only the wake-up circuit is powered on |
| G3 | Mechanical off. All power supply failures |

12.3. Description of Registers

This section describes the power management related registers. The register voltage field indicates the voltage field to which this bit of the register belongs.

PMCON_SOC: SOC General PM Configuration Register

Table 177. SOC general PM configuration register

| Address Offset | Voltage Field | Attribute |
|----------------|---------------|-----------|
|----------------|---------------|-----------|

| 0x00 | | SOC | R/W, RO |
|-----------|--|-----|---------|
| Bit Field | Description | | |
| 25 | PWRBTN_LVL - RO This bit indicates the current PWRBTNn signal status. | | |
| 24 | PWRTYP - RO This bit indicates the power supply mode. 1 : AC (Adapter) 0 : Battery | | |
| 23:0 | Reserved | | |

PMCON_RESUME : RESUME General PM Configuration Register

Table 178. RESUME general PM configuration register

| Address Offset | | Voltage Field | Attribute |
|----------------|---|---------------|---------------|
| 0x04 | | RESUME | R/W, RO, R/WC |
| Bit Field | Description | | |
| 31:14 | Reserved | | |
| 13 | VSB_GATEn_EN - R/W Enables or disables the VSB_GATEn function. 0 : off; 1 : enable. If RSMRSTn is active, this bit is 1 . This bit is configured by the system after re-powering. If the motherboard uses the VSB_GATEn pin as the power management control signal, the system software must write 1 to this bit. | | |
| 12:11 | VSB_GATEn_DLY - R/W Used to control the duration of the VSB_GATEn signal relative to S3n from S0 to S3 and S3 to S0 (the time advanced when sleeping and the time delayed when waking up). 2' b00 : 31.25ms advance at hibernation and 125ms delay at wake-up. 2' b01 : 62.5ms advance at hibernation, 250ms delay at wake-up. 2' b10 : 125ms advance on hibernation and 500ms delay on wake-up. 2' b11 : 250ms ahead of hibernation and 1s behind wake-up. This field is 2' b0 if RSMRSTn is valid, and is configured by the system after re-powering. | | |
| 10:8 | Reserved | | |

| | |
|---|--|
| 7 | USB_GMAC_OK - R/W If RSMRSTn is valid, this bit is 0 , indicating that USB and GMAC are not configured and cannot wake up the system. The system will configure this bit after re-powering. |
| 6 | CTT_STS - R/WC The system enters the G2/S5 state when a temperature trip occurs in the S0 state, and this bit is used to detect the logged event status after re-powering the system. |
| 5 | CTT_EN - R/W Enable the temperature trip protection mechanism. |
| 4 | LID_OPEN - RO Display status detection bit. 1 : Display is on. 0 : Display is off. |
| 3 | Reserved |
| 2 | SRS (System Reset Status) - R/WC 0 : SYS_RESETh has not been pressed 1 : SYS_RESETh has been pressed. This bit should be checked after system reset and clear it accordingly. |
| 1 | PWROK_FLR (PWROK Failure) - R/WC When the system is in the S0 state, the PWROK signal becomes invalid and this bit is set to 1 . Software writes 1 to clear this bit. |
| 0 | DRAM_INIT - R/W This bit does not affect the hardware function, PMON will set this bit to 1 before DRAM initialization, and write 0 to this bit after finishing DRAM initialization, software can use this bit to check if DRAM initialization has been interrupted. |

PMCON_RTC : RTC General PM Configuration Register

Table 179. RTC general PM configuration register

| Address Offset | | Voltage Field | Attribute |
|----------------|-------------|---------------|-----------|
| 0x08 | | RTC | R/W, R/WC |
| Bit Field | Description | | |
| 31:9 | Reserved | | |

| | |
|-----|---|
| 8 | <p>WOL_EN - R/W</p> <p>Controls whether the SLPLANn signal is active when the system is in the low-power state. When the system is in the operating state, SLPLANn is held high.</p> <p>0: SLPLANn is not valid.</p> <p>1: SLPLANn is pulled low if the system is powered by the power supply. If the system is powered by the battery, WOL_BAT_EN determines whether SLPLANn is pulled low.</p> |
| 7 | <p>WOL_BAT_EN - R/W</p> <p>When the system enters a low-power state and is battery powered and WOL_EN is high.</p> <p>0: SLPLANn is invalid.</p> <p>1: SLPLANn is pulled low.</p> |
| 6:5 | <p>S3_ASSERTION_WIDTH - R/W</p> <p>The 2 bits represent the minimum time interval between when the S3n signal is valid and when it is invalid again.</p> <p>11: 1s</p> <p>10: 125ms</p> <p>01: 1ms</p> <p>00: 60us</p> |
| 4:3 | <p>S4_ASSERTION_WIDTH - R/W</p> <p>The 2 bits represent the minimum time interval between when the S4n signal is valid and when it is invalid again.</p> <p>11: 4s</p> <p>10: 2s</p> <p>01: 1s</p> <p>00: 125us</p> |
| 2 | <p>S4_ASSERTION_EN - R/W</p> <p>0: The interval between valid and re-invalidation of the S4n signal is several RTC periods.</p> <p>1: The interval between valid and re-invalidation of the S4n signal is determined by S4_ASSERTION_WIDTH.</p> |

| | |
|---|---|
| 1 | <p>PWR_FLR (Power Failure) - R/WC</p> <p>This bit is in the RTC domain and can only be reset by RTC_RSTn.</p> <p>1 indicates that a power failure has occurred in the system (entering the G3 state), i.e., all power supplies except RTC have failed (RSMRSTn has been active). The software clears this bit by writing 1.</p> |
| 0 | <p>AFTERG3_EN - R/W</p> <p>This bit determines the action of the system after it enters the G3 state and the power is restored.</p> <p>0: The system will automatically revert to the S0 state after power is restored.</p> <p>1: The system will revert to the S5 state, or if the system was in the S4 state when the power failure occurred, the system will revert to the S4 state after power is restored.</p> <p>This bit will be set to 1 by the power button override and thermal trip events.</p> |

PM1_STS : Power Management 1 Status Register

Table 180. Power Management 1 Status Register

| Address Offset | | Voltage Field | Attribute |
|----------------|--|--------------------|---------------|
| 0x0C | | RESUME / RTC / SOC | R/WC |
| Bit Field | Description | | Voltage Field |
| 31:16 | Reserved | | |
| 15 | <p>WAK_STS (Wake Status) - R/WC</p> <p>0: Software writes 1 to clear this bit.</p> <p>1: Hardware writes 1 to this bit if the system is woken up from any of the sleep states by a wakeup event.</p> | | Resume |
| 14 | <p>PCIEXP_WAKE_STS - R/WC</p> <p>1: PCIE wake-up event occurs</p> <p>0: Software write 1 to clear the bit</p> | | Resume |
| 13:12 | Reserved | | |
| 11 | <p>PRBTNOR_STS (Power Button Override Status) - R/WC</p> <p>0: Software writes 1 to clear this bit.</p> <p>1: When power button override occurs, this bit is set to 1, the system enters G2/S5 unconditionally state, while setting AFTERG3_EN to 1.</p> | | RTC |

| | | |
|-----|---|--------|
| 10 | RTC_STS (RTC Status) - R/WC 0: Software writes 1 to clear this bit. 1: This bit is 1 when the RTC generates an alarm. Also when RTC_EN is valid, this bit generates a wake-up event. | Resume |
| 9 | Reserved | |
| 8 | PWRBTN_STS (Power Button Status) - R/WC 0: Software writes 1 to clear this bit. Thermal trip will clear this bit. 1: This bit will be set to 1 when PWRBTNn is pressed and held for more than 16ms (less than 4s). In the S0 state, an interrupt is generated when both PWRBTN_EN and PWRBTN_STS are active. During any sleep state from S3-S5, the system will resume if PWRBTN_STS is set. | Resume |
| 7:1 | Reserved | |
| 0 | TMROF_STS (PM Timer Overflow Status) - R/WC 0: Software writes 1 to clear this bit. 1: When the highest bit of the 24-bit counter (20ns per clock cycle) is inverted, this bit is set to 1. The timer function is recommended to be done with HPET. | SOC |

PM1_EN: Power Management 1 Enable Register

Table 181. Power management 1 enable register

| Address Offset | | Voltage Field | Attribute |
|----------------|---|----------------|-----------|
| 0x10 | | RESUME/RTC/SOC | R/W |
| Bit Field | Description | Voltage Field | |
| 31:15 | Reserved | | |
| 14 | PCIEXP_WAKE_DIS - R/W When this bit is set, no PCIe wake-up event is generated, but the value of this bit does not affect the value of PCIEXP_WAKE_STS . | resume | |
| 13:11 | Reserved | | |
| 10 | RTC_EN (RTC Event Enable) - R/W RTC wake-up and interrupt enable. | rtc | |
| 9 | Reserved | | |
| 8 | PWRBTN_EN (Power Button Enable) - R/W PWRBTN interrupt event generation enable, this bit does not affect PWRBTN wake-up event generation. | resume | |
| 7:1 | Reserved | | |

| | | |
|---|--|-----|
| 0 | TMROF_EN (PM Timer Overflow Enable) - R/W If this bit is set, TMROF_STS will generate an interrupt. | SOC |
|---|--|-----|

PM1_CNT: Power Management 1 Control Register

Table 182. Power management 1 control register

| Address Offset | | Voltage Field | Attribute |
|----------------|--|----------------|-----------|
| 0x14 | | RESUME/RTC/SOC | R/W |
| Bit Field | Description | Voltage Field | |
| 31:14 | Reserved | | |
| 13 | SLP_EN (Sleep Enable) - R/W Writing 1 to this bit will cause the system to enter the SLP_TYP declared hibernation state, and this bit will automatically revert to 0 upon entering the associated hibernation state. | resume | |
| 12:10 | SLP_TYP (Sleep Type) - R/W This 3 bits indicate the hibernation state of the system. 000: S0 state. 001: Reserved. 010: Reserved. 011: Reserved. 100: Reserved. 101: Suspend-to-RAM. S3n signal is valid, enter S3 state. 110: Suspend-to-Disk. S3n , S4n signals are valid, enter S4 state. 111: Soft Off. S3n , S4n , S5n signals are valid, enter S5 state. | rtc | |
| 9:1 | Reserved | | |
| 0 | INT_EN - R/W Interrupt enable switch to enable the generation of interrupt signals for the power management controller. | SOC | |

PM1_TMR: Power Management 1 Timer

Table 183. Power management 1 timer

| Address Offset | | Voltage Field | Attribute |
|----------------|-------------|---------------|-----------|
| 0x18 | | SOC | RO |
| Bit Field | Description | | |
| 31:24 | Reserved | | |

| | |
|------|---|
| 23:0 | TMR_VAL (Timer Value) - RO Counter counts with a period of 8ns. When the 23 bit is inverted, the TNROF_STS bit is set. HPET is recommended. |
|------|---|

GPE0_STS: General Purpose Event0 Status Register

Table 184. General purpose event0 status register

| Address Offset | | Voltage Field | Attribute |
|----------------|---|---------------|-----------|
| 0x28 | | RESUME | R/WC |
| Bit Field | Description | | |
| 31:16 | Reserved | | |
| 15:10 | USB[5:0]_STS - R/WC Only the bit 10 is meaningful, the 15:11 bits are meaningless for now. 0: Software writes 1 to clear this bit. 1: These bits are set when a USB wake event occurs, and when the USBx_EN bit is valid, a wake event or interrupt is generated. | | |
| 9 | Reserved | | |
| 8 | RI_STS - R/WC 0: Software writes 1 to clear this bit. 1: This bit is set when the RIn signal is valid. | | |
| 7 | BATLOW_STS - R/WC 0: Software writes 1 to clear this bit. 1: This bit is set when the BATLOWn signal is active. If BATLOW_EN is valid, an interrupt will be generated when BATLOW_STS is set. This bit does not generate a wake-up event. | | |
| 6 | GMAC1_STS - R/WC 0: Software writes 1 to clear this bit. 1: These bits are set when a wake event occurs in GMAC1 and generate a wake event or interrupt when the GMAC1_EN bit is valid. | | |
| 5 | GMAC0_STS - R/WC 0: Software writes 1 to clear this bit. 1: These bits are set when a wake event occurs in GMAC0 and generate a wake event or interrupt when the GMAC0_EN bit is valid. | | |

| | |
|---|--|
| 4 | LID_STS - R/WC 0: Software writes 1 to clear this bit. 1: When the LID_EN bit is valid, a wake-up event is generated. |
| 3 | CTW_STS - R/WC Thermal warning is generated. |
| 2 | CTA_STS - R/WC Thermal alert is generated. |
| 1 | PWRSWITCH_STS - R/WC The PWRTYP changes when the power supply status changes. This bit generates an interrupt. |
| 0 | Reserved |

GPE0_EN: General Purpose Event0 Enable Register

Table 185. General purpose event0 enable register

| Address Offset | | Voltage Field | Attribute |
|----------------|--|---------------|---------------|
| 0x2C | | RESUME / RTC | R/W |
| Bit Field | Description | | Voltage Field |
| 31:16 | Reserved | | |
| 15:10 | USB[5 :0]_EN - R/W 0: Invalid. 1: Enable USBx_STS to wake-up event that will generate an interrupt signal when returning to S0. | | |
| 9 | Reserved | | |
| 8 | RI_EN - R/W 0: Invalid. 1: Enable RIn_STS wake-up event that will generate an interrupt signal when returning to S0. | | RTC |
| 7 | BATLOW_EN - R/W 0: Invalid. 1: Enable BATLOWn interrupt event. | | RTC |

| | | |
|---|---|-----|
| 6 | GMAC1_EN - R/W 0: Invalid. 1: Enable GMAC1_STS wake-up event, which will generate an interrupt signal when returning to S0. | RTC |
| 5 | GMAC0_EN - R/W 0: Invalid. 1: Enable GMAC0_STS wake-up event, which will generate an interrupt signal when returning to S0. | |
| 4 | LID_EN - R/W 0: Invalid. 1: Enable LID_STS wake-up event, and an interrupt signal will be generated when S0 state. | |
| 3 | CTW_EN - R/W Enable THERMAL WARNING interrupt. | |
| 2 | CTA_EN - R/W Enable THERMAL ALERT interrupt. | |
| 1 | PWRSWITCH_EN - R/W Enable PWRSWITCH_STS interrupt. | |
| 0 | LID_POL - R/W This bit sets the polarity of the LID . | |

RST_CNT: Reset Control Register

Table 186. Reset control register

| Address Offset | | Voltage Field | Attribute |
|----------------|--|---------------|-----------|
| 0x30 | | SOC | R/W |
| Bit Field | Description | | |
| 31:2 | Reserved | | |
| 1 | WD_EN - R/W Watch dog function enable. | | |
| 0 | OS_RST - R/W Software writes this bit to reset the system. | | |

WD_SET : Watch Dog Set Register

Table 187. Watch dog set register

| Address Offset | Voltage Field | Attribute |
|----------------|--|-----------|
| 0x34 | SOC | WO |
| Bit Field | Description | |
| 31:1 | Reserved | |
| 0 | When WD_EN is 1, writing this bit will refill the internal watch dog counter with the value of WD_Timer . Note that the watch dog counter operates at 50MHz. | |

WD_Timer: Watch Dog Timer Register

Table 188. Watch dog timer register

| Address Offset | Voltage Field | Attribute |
|----------------|--|-----------|
| 0x38 | SOC | R/W |
| Bit Field | Description | |
| 31:0 | The value of this register is the watch dog refill value, and the reset value is all 1s. | |

GEN_RTC_1: General RTC Register 1

Table 189. General RTC register 1

| Address Offset | Voltage Field | Attribute |
|----------------|-------------------------------|-----------|
| 0x50 | RTC | R/W |
| Bit Field | Description | |
| 31:0 | RTC general purpose register. | |

GEN_RTC_2: General RTC Register 2

Table 190. General RTC register 2

| Address Offset | Voltage Field | Attribute |
|----------------|-------------------------------|-----------|
| 0x54 | RTC | R/W |
| Bit Field | Description | |
| 31:0 | RTC general purpose register. | |

Chapter 13. RTC

The Real Time Clock (RTC) unit can be configured when the motherboard is powered up, and when the motherboard is powered down, the unit still operates and can run normally on the on-board battery power alone. The RTC unit operates with only a few microamps of current.

The RTC contains an oscillator, which in combination with an external 32.768KHZ crystal generates the operating clock. This clock is used for time information maintenance and is used to maintain time information and to generate various timing and counting interrupts.

The RTC module contains two counters, the TOY (Time of Year) counter and the RTC counter. The TOY counter counts in years, months, hours, minutes and seconds with an accuracy of 0.1s. The RTC counter counts at 32.768KHz and is 32-bit length.

13.1. Access Address

The base address of accessing the RTC module is the base address of the MISC low-speed device block plus an offset of 0x50100.

Note: The RTC module only supports access by 4 bytes.

The physical address composition of the RTC module internal registers is as follows.

Table 191. The physical address composition of the RTC module internal registers

| Address bits | Composition | Note |
|--------------|-------------|----------------------------|
| [15:9] | 0 | Reserved |
| [8] | 1 | Reserved |
| [7:0] | REG | Internal registers address |

13.2. Description of Registers

Table 192. List of RTC registers

| Name | Offset address | Length | Read/Write | Description |
|---------------|----------------|--------|------------|--|
| sys_toytrim | 0x20 | 32 | R/W | Software must initialize it to 0 |
| sys_toywrite0 | 0x24 | 32 | WO | TOY low 32 bits input |
| sys_toywrite1 | 0x28 | 32 | WO | TOY high 32 bits input |
| sys_toyread0 | 0x2C | 32 | RO | TOY low 32 bits output |
| sys_toyread1 | 0x30 | 32 | RO | TOY high 32 bits output |
| sys_toymatch0 | 0x34 | 32 | R/W | TOY timer interrupt 0 |
| sys_toymatch1 | 0x38 | 32 | R/W | TOY timer interrupt 1 |
| sys_toymatch2 | 0x3C | 32 | R/W | TOY timer interrupt 2 |
| sys_rtctrl | 0x40 | 32 | R/W | TOY and RTC control registers Software must initialize them |
| sys_rtctrim | 0x60 | 32 | R/W | Software must initialize it to 0 |

| Name | Offset address | Length | Read/Write | Description |
|---------------|----------------|--------|------------|-----------------------------|
| sys_rtcwrite0 | 0x64 | 32 | WO | RTC timer counter input |
| sys_rtcread0 | 0x68 | 32 | RO | RTC timer counter output |
| sys_rtcmatch0 | 0x6C | 32 | R/W | RTC clock timer interrupt 0 |
| sys_rtcmatch1 | 0x70 | 32 | R/W | RTC clock timer interrupt 1 |
| sys_rtcmatch2 | 0x74 | 32 | R/W | RTC clock timer interrupt 2 |

13.2.1. SYS_TOYWRITE0

Address Offset: 24-27h

Attribute: WO

Default value: N/A

Size: 4

Table 193. SYS_TOYWRITE0

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|-----------------------|
| 31:26 | TOY_MONTH | WO | Month, range 1-12 |
| 25:21 | TOY_DAY | WO | Day, range 1-31 |
| 20:16 | TOY_HOUR | WO | Hour, range 0-23 |
| 15:10 | TOY_MIN | WO | Minute, range 0-59 |
| 9:4 | TOY_SEC | WO | Second, range 0-59 |
| 3:0 | TOY_MILLISEC | WO | 0.1 Second, range 0-9 |

13.2.2. SYS_TOYWRITE1

Address Offset: 28-2Bh

Attribute: WO

Default value: N/A

Size: 4

Table 194. SYS_TOYWRITE1

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---------------------|
| 31:0 | TOY_YEAR | WO | Year, range 0-16383 |

13.2.3. SYS_TOYREAD0

Address Offset: 2C-2Fh

Attribute: RO

Default value: 00000000h

Size: 4

Table 195. SYS_TOYREAD0

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|-----------------------|
| 31:26 | TOY_MONTH | RO | Month, range 1-12 |
| 25:21 | TOY_DAY | RO | Day, range 1-31 |
| 20:16 | TOY_HOUR | RO | Hour, range 0-23 |
| 15:10 | TOY_MIN | RO | Minute, range 0-59 |
| 9:4 | TOY_SEC | RO | Second, range 0-59 |
| 3:0 | TOY_MILLISEC | RO | 0.1 Second, range 0-9 |

13.2.4. SYS_TOYREAD1

Address Offset: 30-33h

Attribute: RO

Default value: 00000000h

Size: 4

Table 196. SYS_TOYREAD1

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---------------------|
| 31:0 | TOY_YEAR | RO | Year, range 0-16383 |

13.2.5. SYS_TOYMATCH0

Address Offset: 34-37h

Attribute: R/W

Default value: 00000000h

Size: 4

Table 197. SYS_TOYMATCH0

| Bit Field | Name | Read/Write | Description |
|-----------|-------|------------|---------------------|
| 31:26 | YEAR | R/W | Year, range 0-16383 |
| 25:22 | MONTH | R/W | Month, range 1-12 |
| 21:17 | DAY | R/W | Day, range 1-31 |
| 16:12 | HOUR | R/W | Hour, range 0-23 |
| 11:6 | MIN | R/W | Minute, range 0-59 |

| Bit Field | Name | Read/Write | Description |
|-----------|------|------------|--------------------|
| 5:0 | SEC | R/W | Second, range 0-59 |

13.2.6. SYS_TOYMATCH1

Address Offset: 38-3Bh

Attribute: R/W

Default value: 00000000h

Size: 4

Table 198. SYS_TOYMATCH1

| Bit Field | Name | Read/Write | Description |
|-----------|-------|------------|---------------------|
| 31:26 | YEAR | R/W | Year, range 0-16383 |
| 25:22 | MONTH | R/W | Month, range 1-12 |
| 21:17 | DAY | R/W | Day, range 1-31 |
| 16:12 | HOUR | R/W | Hour, range 0-23 |
| 11:6 | MIN | R/W | Minute, range 0-59 |
| 5:0 | SEC | R/W | Second, range 0-59 |

13.2.7. SYS_TOYMATCH2

Address Offset: 3C-3Fh

Attribute: R/W

Default value: 00000000h

Size: 4

Table 199. SYS_TOYMATCH2

| Bit Field | Name | Read/Write | Description |
|-----------|-------|------------|---------------------|
| 31:26 | YEAR | R/W | Year, range 0-16383 |
| 25:22 | MONTH | R/W | Month, range 1-12 |
| 21:17 | DAY | R/W | Day, range 1-31 |
| 16:12 | HOUR | R/W | Hour, range 0-23 |
| 11:6 | MIN | R/W | Minute, range 0-59 |
| 5:0 | SEC | R/W | Second, range 0-59 |

13.2.8. SYS_RTCCTRL

Address Offset: 40-43h

Attribute: RO, R/W

Default value: 00000000h

Size: 4

Table 200. SYS_RTCCTRL

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---|
| 31:24 | Reserved | RO | Reserved |
| 23 | ERS | RO | REN (bit 13) write status |
| 22:21 | Reserved | RO | Reserved |
| 20 | RTS | RO | Sys_rtctrim write status |
| 19 | RM2 | RO | Sys_rtcmatch2 write status |
| 18 | RM2 | RO | Sys_rtcmatch2 write status |
| 17 | RM0 | RO | Sys_rtcmatch0 write status |
| 16 | RS | RO | Sys_rtcwrite write status |
| 15:14 | Reserved | RO | Reserved |
| 13 | REN | R/W | RTC enable (active high). Needs to be initialized to 1 |
| 12 | Reserved | RO | Reserved |
| 11 | TEN | R/W | TOY enable (active high). Needs to be initialized to 1 |
| 10:9 | Reserved | RO | Reserved |
| 8 | EO | R/W | 0: 32.768k crystal oscillation disable 1: 32.768k crystal oscillation enable |
| 7:6 | Reserved | RO | Reserved |
| 5 | Status | RO | 32K crystal oscillation work state. 0: 32.768k crystal oscillation not work 1: 32.768k crystal oscillation working properly |
| 4 | Reserved | RO | Reserved |
| 3 | TM2 | RO | Sys_toymatch2 write state |
| 2 | TM1 | RO | Sys_toymatch1 write state |
| 1 | TM0 | RO | Sys_toymatch0 write state |
| 0 | TS | RO | Sys_toywrite write state |

13.2.9. SYS_RTCWRITE

Address Offset: 64-67h

Attribute: WO

Default value: N/A

Size: 4

Table 201. SYS_RTCWRITE

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|----------------------------|
| 31 : 0 | RTCWRITE | WO | RTC counter input register |

13.2.10. SYS_RTCREAD

Address Offset: 68-6Bh

Attribute: RO

Default value: 00000000h

Size: 4

Table 202. SYS_RTCREAD

| Bit Field | Name | Read/Write | Description |
|-----------|---------|------------|-----------------------------|
| 31 : 0 | RTCREAD | RO | RTC counter output register |

13.2.11. SYS_RTCMATCH0

Address Offset: 6C-6Fh

Attribute: R/W

Default value: 00000000h

Size: 4

Table 203. SYS_RTCMATCH0

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---------------------------------|
| 31 : 0 | RTCMATCH0 | R/W | RTC timer comparison register 0 |

13.2.12. SYS_RTCMATCH1

Address Offset: 70-73h

Attribute: R/W

Default value: 00000000h

Size: 4

Table 204. SYS_RTCMATCH1

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---------------------------------|
| 31 : 0 | RTCMATCH1 | R/W | RTC timer comparison register 1 |

13.2.13. SYS_RTCMATCH2

Address Offset: 74-77h

Attribute: R/W

Default value: 00000000h

Size: 4

Table 205. SYS_RTCMATCH2

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---------------------------------|
| 31 : 0 | RTCMATCH2 | R/W | RTC timer comparison register 2 |

Chapter 14. GPIO

The bridge chip has 57 GPIO pins, **GPIO00** is a dedicated GPIO pin, and the remaining 56 are multiplexed with other functions. Each GPIO pin is controlled by a set of control registers, including: GPIO direction control (**GPIO_OEN**), GPIO output (**GPIO_O**), GPIO input (**GPIO_I**), and GPIO input interrupt enable control (**GPIO_INT_EN**).

Table 206. GPIO control register

| Register | Size (bit) | Description |
|--------------------|------------|----------------------------------|
| GPIO_OEN | 1 | GPIO output enable (active low). |
| GPIO_O | 1 | GPIO output. |
| GPIO_I | 1 | GPIO input. |
| GPIO_INT_EN | 1 | GPIO interrupt enable. |

14.1. Access Address

The base address of accessing the GPIO module is the base address of the MISC low-speed device block plus an offset of **0x60000**.

Note: The GPIO module only supports access by 1 byte.

The bridge chip provides two ways to control the GPIO pins. One is to control each GPIO pin by bit and the other is to control each GPIO pin by byte. The bridge chip does this by providing two address spaces to map the GPIO control registers. One is a per-bit mapping and the other is a per-byte indexing of each bit of the control register. Correspondingly, the GPIO internal address space is divided into two parts.

The latter way is recommended for the GPIO controller pins.

The physical address composition of the GPIO module internal registers is as follows.

Table 207. The physical address composition of the GPIO module internal registers

| Address space | Description |
|--------------------|----------------------------------|
| 0x800-0xC00 | Address of byte control register |
| 0x0-0x40 | Address of bit control register |

Table 208. Address of GPIO bit control configuration register

| Address Offset | Register | Size (bit) | Description |
|----------------|--------------------|------------|--|
| 0x00 | GPIO_OEN | 57 | GPIO output enable (active low). Each bit controls one GPIO pin. |
| 0x10 | GPIO_O | 57 | GPIO output. Each bit controls one GPIO pin. |
| 0x20 | GPIO_I | 57 | GPIO input. Each bit controls one GPIO pin. |
| 0x30 | GPIO_INT_EN | 57 | GPIO interrupt enable. Each bit controls one GPIO pin. |

Table 209. Address of GPIO byte control configuration register

| Address Offset | Register | Size (bit) | Description |
|----------------|-------------|------------|---|
| 0x800 | GPIO_OEN | 57 | GPIO output enable (active low). Each byte controls one GPIO pin, bit 0 is valid. |
| 0x900 | GPIO_O | 57 | GPIO output. Each byte controls one GPIO pin, bit 0 is valid. |
| 0xA00 | GPIO_I | 57 | GPIO input. Each byte controls one GPIO pin, bit 0 is valid. |
| 0xB00 | GPIO_INT_EN | 57 | GPIO interrupt enable. Each byte controls one GPIO pin, bit 0 is valid. |

For example, the output input direction of **GPIO03** can be controlled either by **bit[3]** with offset address **0x0** (taking care not to affect other bits) or by a byte with offset address **0x803** (only **bit[0]** is valid).

14.2. Description of Registers

GPIO Direction Control

Address Offset: **00-03h**

Attribute: R/W

Default value: **FFFFFFFF0h**

Size: **4**

Table 210. GPIO direction control

| Bit Field | Name | Read/Write | Description |
|-------------|-----------------|------------|--|
| 31:0 | GPIO_OEN | R/W | Corresponds to the direction control of GPIO[31:0] . 0 : Output 1 : Input |

Address Offset: **04-07h**

Attribute: R/W

Default value: **FFFFFFFFh**

Size: **4**

Table 211. GPIO direction control

| Bit Field | Name | Read/Write | Description |
|--------------|-----------------|------------|-------------|
| 31:26 | Reserved | R/W | Reserved. |

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---|
| 25:0 | GPIO_OEN | R/W | Corresponds to the direction control of GPIO[57:32]. 0: Output 1: Input |

GPIO Output

Address Offset: 00-03h

Attribute: R/W

Default value: 000000Fh

Size: 4

Table 212. GPIO output

| Bit Field | Name | Read/Write | Description |
|-----------|--------|------------|--|
| 31:0 | GPIO_0 | R/W | Corresponds to the output of GPIO[31:0]. |

Address Offset: 04-07h

Attribute: R/W

Default value: 00000000h

Size: 4

Table 213. GPIO output

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---|
| 31:26 | Reserved | R/W | Reserved. |
| 25:0 | GPIO_0 | R/W | Corresponds to the output of GPIO[57:32]. |

GPIO Input

Address Offset: 00-03h

Attribute: RO

Default value: N/A

Size: 4

Table 214. GPIO input

| Bit Field | Name | Read/Write | Description |
|-----------|--------|------------|---|
| 31:0 | GPIO_I | RO | Corresponds to the input of GPIO[31:0]. |

Address Offset: 04-07h

Attribute: RO

Default value: 00000000h

Size: 4

Table 215. GPIO input

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|--|
| 31:26 | Reserved | R/W | Reserved. |
| 25:0 | GPIO_I | RO | Corresponds to the input of GPIO[57:32]. |

GPIO Interrupt Enable

Address Offset: 00-03h

Attribute: R/W

Default value: 00000000h

Size: 4

Table 216. GPIO interrupt enable

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|---|
| 31:0 | GPIO_OEN | R/W | Corresponds to the interrupt enable of GPIO[31:0]. 0: Disable interrupt 1: Enable interrupt |

Address Offset: 04-07h

Attribute: R/W

Default value: 00000000h

Size: 4

Table 217. GPIO interrupt enable

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|--|
| 31:26 | Reserved | R/W | Reserved. |
| 25:0 | GPIO_OEN | R/W | Corresponds to the interrupt enable of GPIO[57:32]. 0: Disable interrupt 1: Enable interrupt |

Chapter 15. GMAC Controller (D3:F0, D3:F1)

The bridge integrates two GMAC controllers, which have the same functions.

Note: See [Notes on the Use of the Software](#) for software enablement of 64-bit DMA for the GMAC controllers.

15.1. GMAC Configuration Register (D3:F0, D3:F1)

Table 218. GMAC controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|-------------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A03h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 00h | RO |
| 0Bh | BCC | Base Class Code | 02h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 80h | RO |
| 10h-17h | CNL_BAR | Control Block Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note: Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (GMAC - D3:F0, D3:F1)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 219. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 15:2 | Reserved | RO | Reserved. |
| 1 | Memory Space Enable | R/W | This bit is used to control whether access to the GMAC control registers is enabled. 0: Disable access. 1: Enable access to the GMAC control registers. The BAR register must be configured before this bit can be configured to 1. |
| 0 | Reserved | RO | Reserved. |

CNL_BAR - Control Base Address Register

This register is used to configure the base address of the control registers of the GMAC controller.

Address Offset: 10-13h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 220. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 31:15 | Base Address | RW | The software writes to this register field the low address of the base address allocated to the GMAC control register. |
| 14:4 | Memory Size | RO | The address space size of GMAC control register is 32KB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 14-17h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 221. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:0 | Base Address | RW | The software writes to this register field the high 32-bit address of the base address allocated to the GMAC control register. |

Chapter 16. USB Controller (D4:F0/1, D5:F0/1)

The bridge contains two USB controllers, each containing three ports.

The USB ports of the bridge have the following features.

- Compatible with USB Rev 1.1, USB Rev 2.0 protocols
- Compatible with OHCI Rev 1.0, EHCI Rev 1.0 protocols
- Supports LS (Low Speed), FS (Full Speed) and HS (High Speed) USB devices
- Works in Host mode, OTG mode is not supported

Each USB controller module of the bridge includes an EHCI controller and an OHCI controller, with each EHCI controller and OHCI controller supporting 3 ports. The EHCI controller is used by default, and control is transferred to the OHCI controller only when the hooked up device is a full-speed or low-speed device. When a full-speed or low-speed device is unplugged, control is returned to the EHCI controller.

Note: The **Memory Space Enable** control for the OHCI and EHCI device headers of USB devices requires special handling, see [Notes on the Use of the Software](#).

16.1. EHCI Controller

16.1.1. EHCI Configuration Register (D4:F1, D5:F1)

Table 222. USB-EHCI controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|-------------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A14h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 20h | RO |
| 0Ah | SCC | Sub Class Code | 03h | RO |
| 0Bh | BCC | Base Class Code | 0Ch | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 80h | RO |
| 10h-17h | CNL_BAR | Control Block Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note: Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (USB EHCI - D4:F1, D5:F1)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 223. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 15:2 | Reserved | RO | Reserved. |
| 1 | Memory Space Enable | R/W | <p>This bit is used to control whether access to the USB EHCI control registers is enabled.</p> <p>0: Disable access.</p> <p>1: Enable access to the USB EHCI control registers. The BAR register must be configured before this bit can be configured to 1.</p> <p>In rev. 00, this bit controls the Memory Space Enable of the OHCI. The Memory Space Enable of the EHCI is controlled by the corresponding bit of the OHCI controller.</p> |
| 0 | Reserved | RO | Reserved. |

CNL_BAR - Control Base Address Register

This register is used to configure the base address of the control registers of the EHCI controller.

Address Offset: 10-13h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 224. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 31:15 | Base Address | RW | The software writes to this register field the low address of the base address allocated to the EHCI control register. |
| 14:4 | Memory Size | RO | The address space size of EHCI control register is 32KB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |

| Bit Field | Name | Read/Write | Description |
|-----------|-------------------|------------|--|
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 14-17h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 225. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:0 | Base Address | RW | Software writes to this register field the high 32-bit address of the base address allocated to the EHCI control register. |

The bridge's USB host controller is compatible with the EHCI Rev 1.0 protocol. Refer to the Enhanced Host Controller Interface Rev 1.0 Specification for details of the Capability register and Operational register.

16.2. OHCI Controller

16.2.1. OHCI Configuration Register (D4:F0, D5:F0)

Table 226. USB-OHCI controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|-------------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A24h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 10h | RO |
| 0Ah | SCC | Sub Class Code | 03h | RO |
| 0Bh | BCC | Base Class Code | 0Ch | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 80h | RO |
| 10h-17h | CNL_BAR | Control Block Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note: Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (USB OHCI - D4:F0, D5:F0)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 227. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 15:2 | Reserved | RO | Reserved. |
| 1 | Memory Space Enable | R/W | This bit is used to control whether access to the USB OHCI control registers is enabled. 0: Disable access. 1: Enable access to the USB OHCI control registers. The BAR register must be configured before this bit can be configured to 1. In rev. 00, this bit controls the Memory Space Enable of the EHCI. The Memory Space Enable of the OHCI is controlled by the corresponding bit of the EHCI controller. |
| 0 | Reserved | RO | Reserved. |

CNL_BAR - Control Base Address Register

This register is used to configure the base address of the control registers of the OHCI controller.

Address Offset: 10-13h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 228. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:15 | Base Address | RW | The software writes to this register field the low address of the base address allocated to the OHCI control register. |
| 14:4 | Memory Size | RO | The address space size of OHCI control register is 32KB. |

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 14-17h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 229. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:0 | Base Address | RW | Software writes to this register field the high 32-bit address of the base address allocated to the OHCI control register. |

The bridge's USB host controller is compatible with the OHCI Rev 1.0 protocol. Refer to the Open Host Controller Interface Rev 1.0 Specification for details of the operational registers.

Chapter 17. Graphics Processor (D6:F0)

17.1. GPU Configuration Register (D6:F0)

Table 230. GPU controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|--------------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A15h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 02h | RO |
| 0Bh | BCC | Base Class Code | 03h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 80h | RO |
| 10h-17h | CNL_BAR | Control Block Base Address Register | 0000000000000004h | R/W, RO |
| 18h-1Fh | GMEM_BAR | Graphic Memory Base Address Register | 0000000000000004h | R/W, RO |
| 27h-20h | RSV_BAR | Reserved Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note: Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (GPU - D6:F0)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 231. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 15:2 | Reserved | RO | Reserved. |

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 1 | Memory Space Enable | R/W | This bit is used to control whether access to the GPU control registers is enabled. 0: Disable access. 1: Enable access to the GMAC control registers and GMEN space. The BAR register must be configured before this bit can be configured to 1. |
| 0 | Reserved | RO | Reserved. |

CNL_BAR - Control Base Address Register

This register is used to configure the base address of the control registers of the GMAC controller.

Address Offset: 10-13h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 232. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 31:18 | Base Address | RW | Software writes to this register field the low address of the base address allocated to the GPU control register. |
| 17:4 | Memory Size | RO | The address space size of the GPU control registers is 32KB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 14-17h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 233. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 31:0 | Base Address | RW | Software writes to this register field the high 32-bit address of the base address allocated to the GPU control register. |

GMEM_BAR - Video Memory Base Address Register

This register is used to configure the base address of the video memory.

Address Offset: 18-1Bh

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 234. Video memory base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 31:X | Base Address | RW | The software writes to this register field the low bit of the base address allocated to the video memory. |
| X:4 | Memory Size | RO | The memory size is configured by the BIOS. The maximum is not more than 512MB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 1C-1Fh

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 235. Video memory base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 31:0 | Base Address | RW | The software writes to this register field the high 32-bit address allocated to the base address of the video memory. |

RSV_BAR - Reserved Window Base Address Register

This register is used to configure the base address of the reserved registers of the GPU controller.

Address Offset: 20-23h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 236. Reserved window base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 31:18 | Base Address | RW | The software writes to this register field the low address of the base address allocated to the GPU reserved register. |
| 17:4 | Memory Size | RO | The address space size of the GPU reserved registers is 256B. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 24-27h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 237. Reserved window base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:0 | Base Address | RW | The software writes to this register field the high 32-bit address of the base address allocated to the GPU reserved register. |

17.2. DDR3 Memory Interface

The bridge chip's integrated memory interface complies with the DDR3 SDRAM standard (JESD79-3).

The bridge supports 1 chip select, 16 row addresses, 15 column addresses, and 3 logical body addresses.

The bridge chip's memory controller has the following characteristics.

- Full-flow operation of commands, read and write data on the interface
- Memory command merging and sorting to improve the overall bandwidth
- Basic parameters of memory devices can be modified
- Supports 133-667MHz clock frequency

Access Address

The DDR3 memory controller consists of two address spaces: the memory space for video memory controller configuration register and the memory space for the video memory. These two address spaces share the same address space (the video memory address space, the address space allocated to GMEM_BAR). The final access to the memory address space is determined by the parameter `disable_gmem_confspace` — bit 3 of general configuration register 0 of the bridge configuration register `addr_0x420[3]`.

When the configuration parameter `disable_gmem_confspace = 0`, all accesses to the memory are configuration register accesses. When the configuration parameter `disable_gmem_confspace = 1`, the accesses to the memory are normal memory read and write accesses.

Chapter 18. Display Controller (D6:F1)

The features supported by the display controller of the bridge include the following.

- Dual DVO interface displays
- Each display supports up to 1920x1080@60Hz
- Two hardware cursors modes: Monochrome, ARGB8888
- Four color depths: RGB444, RGB555, RGB565, RGB888
- Output dithering and gamma correction
- Switchable dual routability frame buffer
- Interrupt and soft reset

18.1. DC Configuration Register (D6:F1)

Table 238. DC controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|-------------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A06h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 03h | RO |
| 0Bh | BCC | Base Class Code | 0Ch | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 80h | RO |
| 10h-17h | CNL_BAR | Control Block Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note: Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (DC - D6:F1)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 239. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 15:2 | Reserved | RO | Reserved. |
| 1 | Memory Space Enable | R/W | This bit is used to control whether access to the DC control registers is enabled. 0: Disable access. 1: Enable access to the DC control registers. The BAR register must be configured before this bit can be configured to 1. |
| 0 | Reserved | RO | Reserved. |

CNL_BAR - Control Base Address Register

This register is used to configure the base address of the control registers of the GMAC controller.

Address Offset: 10-13h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 240. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 31:16 | Base Address | RW | The software writes to this register field the low address of the base address assigned to the DC control register. |
| 15:4 | Memory Size | RO | The address space size of DC control register is 64KB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 14-17h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 241. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 31:0 | Base Address | RW | Software writes to this register field the high 32-bit address of the base address assigned to the DC control register. |

18.2. DC Control Register

18.2.1. Display Detection Register

The 7A bridge contains two sets of I2C bus pins specifically for display detection. These two sets of I2C bus pins need to be emulated by software using GPIO pins. These two sets of GPIO pins differ from the GPIO pins in the MISC in that their control registers are placed in the control register space of the DC. The I2C bus of DVO0 is controlled by **bit[1:0]** of the GPIO register, and the I2C bus of DVO1 is controlled by **bit[3:2]** of the GPIO register. The correspondence between I2C pins and GPIO registers is shown in the following table.

Table 242. Correspondence between the I2C pins of the DVO and the control registers

| Pin Name | GPIO control bit |
|----------|------------------|
| DVO0_SDA | 0 |
| DVO0_SCL | 1 |
| DVO1_SDA | 2 |
| DVO1_SCL | 3 |

Each GPIO control bit is controlled by three registers. The addresses of the GPIO control registers are shown in the following table.

Table 243. DVO's I2C pin control register address

| Register Name | Address Offset | Read/Write | Description | Reset Value |
|---------------|----------------|---|---------------------------------|---------------|
| GPIO_OUT | 0x1650 | WO | Output register | 0h |
| GPIO_IN | 0x1650 | RO | Input register | N/A |
| GPIO_EN | 0x1660 | R/W | GPIO direction control register | 0h |
| GPIO_OUT | Bit | Description | | Initial Value |
| DVO0_SDA_OUT | 0 | Control the output value of the DVO0_SDA pin (write only) | | 0 |
| DVO0_SCL_OUT | 1 | Control the output value of the DVO0_SCL pin (write only) | | 0 |
| DVO1_SDA_OUT | 2 | Control the output value of the DVO1_SDA pin (write only) | | 0 |
| DVO1_SCL_OUT | 3 | Control the output value of the DVO1_SCL pin (write only) | | 0 |
| GPIO_IN | Bit | Description | | Initial Value |
| DVO0_SDA_IN | 0 | Control the input value of the DVO0_SDA pin (read only) | | N/A |

| | | | |
|-------------|-----|--|---------------|
| DV00_SCL_IN | 1 | Control the input value of the DV00_SCL pin (write only) | N/A |
| DV01_SDA_IN | 2 | Control the input value of the DV01_SDA pin (write only) | N/A |
| DV01_SCL_IN | 3 | Control the input value of the DV01_SCL pin (write only) | N/A |
| | | | |
| GPIO_EN | Bit | Description | Initial Value |
| DV00_SDA_EN | 0 | Control the direction of the DV00_SDA pin (read/write) | 0 |
| DV00_SCL_EN | 1 | Control the direction of the DV00_SCL pin (read/write) | 0 |
| DV01_SDA_EN | 2 | Control the direction of the DV01_SDA pin (read/write) | 0 |
| DV01_SCL_EN | 3 | Control the direction of the DV01_SCL pin (read/write) | 0 |

Chapter 19. HDA Controller (D7:F0)

The HDA controller is compatible with High Definition Audio Specification Revision 1.0a.

See [PLL1 Configuration Register](#) for HDA-related pin setup registers.

19.1. HDA Configuration Register (D7:F0)

Table 244. HDA controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|-------------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A07h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 03h | RO |
| 0Bh | BCC | Base Class Code | 04h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 00h | RO |
| 10h-17h | CNL_BAR | Control Block Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note:

1. The HDA configuration header is only visible when the relevant pin is configured for HDA mode.
2. Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (HDA - D7:F0)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 245. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 15:2 | Reserved | RO | Reserved. |
| 1 | Memory Space Enable | R/W | This bit is used to control whether access to the HDA control registers is enabled. 0: Disable access. 1: Enable access to the HDA control registers. The BAR register must be configured before this bit can be configured to 1. |
| 0 | Reserved | RO | Reserved. |

CNL_BAR - Control Base Address Register

This register is used to configure the base address of the HDA controller's control registers.

Address Offset: 10-13h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 246. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 31:16 | Base Address | RW | Software writes to this register field the low address of the base address assigned to the HDA control register. |
| 15:4 | Memory Size | RO | The HDA control register has an address space size of 64KB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 14-17h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 247. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:0 | Base Address | RW | The software writes to this register field the high 32-bit address assigned to the base address of the HDA control register. |

19.2. Description of HDA Control Register

The HDA control registers are designed in full accordance with the HD audio Rev 1.0 specification. The following table lists the main register parameters.^[1] Refer to the HD audio Rev 1.0 manual for details.

¹. Translator's note: The original table is missing.

Chapter 20. AC97 Controller (D7:F1)

20.1. AC97 Configuration Register (D7:F1)

Table 248. AC97 controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|-------------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A17h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 01h | RO |
| 0Bh | BCC | Base Class Code | 04h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 00h | RO |
| 10h-17h | CNL_BAR | Control Block Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note:

1. The AC97 configuration header is only visible when the relevant pin is configured for AC97 mode.
2. Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (AC97 - D7:F1)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 249. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 15:2 | Reserved | RO | Reserved. |

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 1 | Memory Space Enable | R/W | This bit is used to control whether access to the AC97 control registers is enabled. 0: Disable access. 1: Enable access to the AC97 control registers. The BAR register must be configured before this bit can be configured to 1. |
| 0 | Reserved | RO | Reserved. |

CNL_BAR - Control Base Address Register

This register is used to configure the base address of the control registers of the AC97 control register.

Address Offset: 10-13h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 250. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 31:16 | Base Address | RW | The software writes to this register field the low address of the base address allocated to the AC97 control register. |
| 15:4 | Memory Size | RO | The address space size of AC97 control register is 64KB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 14-17h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 251. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:0 | Base Address | RW | The software writes to this register field the high 32-bit address of the base address allocated to the AC97 control register. |

20.2. AC97 Controller Register

Table 252. List of AC97 control registers

| Address Offset | Abbreviation | Description | Default Value | Read/Write |
|----------------|--------------|-------------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A17h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 01h | RO |
| 0Bh | BCC | Base Class Code | 04h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 00h | RO |
| 10h-17h | CNL_BAR | Control Block Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

CSR Register

Offset address: 0x00

Reset value: 0x00000000

Table 253. CSR register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|-----------|--------|------------|--|
| 31:2 | Reserved | 30 | RO | Reserved. |
| 1 | RESUME | 1 | R/W | <p>Hanging. Read this bit to return the current state of the AC97 subsystem.</p> <p>1: AC97 subsystem hanged</p> <p>0: Normal operating state</p> <p>Writing 1 to this bit in the pending state will start the recovery operation.</p> |
| 0 | RST_FORCE | 1 | W | <p>AC97 cold boot.</p> <p>Writing 1 will cause the AC97 Codec to cold boot.</p> |

OCC Register

Offset address: 0x04

Reset value: 0x00004141

Table 254. OCC register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|-----------|--------|------------|--|
| 31:24 | Reserved | 10 | R/W | Reserved. |
| 23:16 | Reserved | 10 | R/W | Reserved. |
| 15:10 | OC1_CFG_R | 10 | R/W | Output channel 1: Right channel configuration. |
| 7:0 | OC0_CFG_L | 10 | R/W | Output channel 0: Left channel configuration. |

ICC Register

Offset address: 0x10

Reset value: 0x00410000

Table 255. ICC register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------------|--------|------------|---|
| 31:24 | Reserved | 10 | R/W | Reserved. |
| 23:16 | IC_CFG_MIC | 10 | R/W | Input channel 2: MIC channel configuration. |
| 15:10 | Reserved | 10 | R/W | Reserved. |
| 7:0 | Reserved | 10 | R/W | Reserved. |

Table 256. Description of the sound channel format

| Bit Field | Name | Length | Read/Write | Description | | |
|-----------|------------|--------|------------|--|----------------|---------------|
| 7 | Reserved | 1 | R/W | Reserved. | | |
| 6 | DMA_EN | 1 | R/W | DMA enable. 1: DMA enable. 0: DMA disable. | | |
| 5:4 | FIFO_THRES | 2 | R/W | FIFO threshold | | |
| | | | | 5:4 | Output channel | Input channel |
| | | | | 00 | FIFO 1/4 empty | FIFO 1/4 full |
| | | | | 01 | FIFO 1/2 empty | FIFO 1/2 full |
| | | | | 10 | FIFO 3/4 empty | FIFO 3/4 full |
| | | | | 11 | FIFO empty | FIFO full |

| Bit Field | Name | Length | Read/Write | Description |
|-----------|-------|--------|------------|--|
| 3:2 | SW | 2 | R/W | Number of sampling bits 00: 10 bits 10: 16 bits |
| 1 | VSR | 1 | R/W | Sampling rate 1: Variable sampling rate 0: Fixed sampling rate (410KHz) |
| 0 | CH_EN | 1 | R/W | Channel enable 1: Channel enable 0: Channel disable (or go to energy-saving state) |

Codec Register Access Command

Offset address: 0x110

Reset value: 0x00000000

Table 257. Codec register access command

| Bit Field | Name | Length | Read/Write | Description |
|-----------|-----------|--------|------------|--|
| 31 | CODEC_WR | 1 | R/W | Read/write selection 1: Read. When reading data, first set CODEC_WR to read mode, and set the register address you want to access in CODEC_ADR. Wait until the return data completes interrupt and then read the CODEC_DAT register to read the value. 0: Write. |
| 30:23 | Reserved | 10 | R | Reserved. |
| 22:16 | CODEC_ADR | 7 | R/W | Codec register address |
| 15:0 | CODEC_DAT | 16 | R/W | Codec register data |

Interrupt Status Register/Interrupt Mask Register

Offset address: 0x54/510

Reset value: 0x00000000

Table 258. Interrupt Status Register/Interrupt Mask Register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|---------|--------|------------|----------------------------|
| 31 | IC_FULL | 1 | R/W | Input channel 2: FIFO full |

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------------|--------|------------|--|
| 30 | IC_TH_INT | 1 | R/W | Input channel 2: FIFO reaches threshold |
| 29:10 | Reserved | 22 | R/W | Reserved. |
| 7 | OC1_FULL | 1 | R/W | Output channel 1: FIFO full |
| 6 | OC1_EMPTY | 1 | R/W | Output channel 1: FIFO empty |
| 5 | OC1_TH_INT | 1 | R/W | Output channel 1: FIFO reaches threshold |
| 4 | OC0_FULL | 1 | R/W | Output channel 0: FIFO full |
| 3 | OC0_EMPTY | 1 | R/W | Output channel 0: FIFO empty |
| 2 | OC0_TH_INT | 1 | R/W | Output channel 0: FIFO reaches threshold |
| 1 | CW_DONE | 1 | R/W | Codec register write complete |
| 0 | CR_DONE | 1 | R/W | Codec register read complete |

Interrupt Status/Clear Register

Offset address: 0x5c

Reset value: 0x00000000

Table 259. Interrupt status/clear register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|---------|--------|------------|--|
| 31:0 | INT_CLR | 32 | RO | After masking the interrupt status register, a read of this register will clear all interrupt status in register 0x54. |

OC Interrupt Clear Register

Offset address: 0x60

Reset value: 0x00000000

Table 260. OC interrupt clear register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------------|--------|------------|---|
| 31:0 | INT_OC_CLR | 32 | RO | A read operation of this register will clear the bits[7:2] corresponding to the interrupt status of all output channels in register 0x54. |

IC Interrupt Clear Register

Offset address: 0x64

Reset value: 0x00000000

Table 261. IC interrupt clear register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------------|--------|------------|---|
| 31:0 | INT_IC_CLR | 32 | RO | A read operation of this register will clear the bits[31:30] corresponding to the interrupt status of all input channels in register 0x54 . |

CODEC WRITE Interrupt Clear Register

Offset address: **0x610**

Reset value: **0x00000000**

Table 262. CODEC WRITE interrupt clear register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------------|--------|------------|--|
| 31:0 | INT_CW_CLR | 32 | RO | A read operation of this register will clear the bit[1] in register 0x54 . |

CODEC READ Interrupt Clear Register

Offset address: **0x6c**

Reset value: **00000000h**

Table 263. CODEC READ interrupt clear register

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------------|--------|------------|--|
| 31:0 | INT_CR_CLR | 32 | RO | A read operation of this register will clear the bit[0] in register 0x54 . |

DMA Command Register

This register is used to control the internal DMA controller of the AC97. The DMA controller is described in detail in the following section.

Offset address: **0x100**

Reset value: **00000000h**

Table 264. DMA command register

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---|
| 63:5 | ask_addr | R/W | bit[63:5] of the DMA descriptor address, the lower 5 bits are 0 . |
| 5 | Reserved | R/W | Reserved. |
| 4 | dma_stop | R/W | Stop DMA operation. The DMA controller stops when it has completed reading or writing the current data. |
| 3 | dma_start | R/W | Start DMA operation. The DMA controller reads the descriptor address (ask_addr) and then clears some bits to zero. |

| Bit Field | Name | Read/Write | Description |
|-----------|-----------|------------|---|
| 2 | ask_valid | R/W | The DMA working register is written back to the memory pointed to by (ask_addr) and cleared to zero when finished. |
| 1 | Reserved | R/W | Reserved. |
| 0 | dma_64bit | R/W | DMA controller 64-bit address support. |

20.3. DMA Controller

20.3.1. Description of DMA Controller Structure

The bridge contains 2 DMA controllers for data migration between memory and AC97, which can save resources and improve the efficiency of system data transfer. This saves resources and improves the efficiency of system data transfer.

The process of transporting data by DMA consists of three stages.

1. Pre-processing before transport: The CPU configures the registers related to the DMA descriptor.
2. Data transport: done automatically under the control of the DMA controller.
3. End-of-transport processing: sending an interrupt request.

This DMA controller is limited to data handling in words (4-byte).

The DMA controller supports 64-bit address space, which is mainly controlled by **dma_64bit**. When this bit is set to **1**, it means that the DMA controller works in 64-bit address space, and vice versa for 32-bit address space. In 64-bit address mode, it is necessary to extend **DMA_ORDER_ADDR** and **DMA_SADDR** to 64-bit registers.

20.3.2. DMA Descriptor

DMA_ORDER_ADDR_LOW

Offset address: **0x0**

Reset value: **0x00000000**

Table 265. **DMA_ORDER_ADDR_LOW**

| Bit Field | Name | Length | Read/Write | Description |
|-------------|----------------|-----------|------------|---|
| 31:1 | dma_order_addr | 31 | R/W | Memory internal next descriptor address register (low 32 bits). |
| 0 | Dma_order_en | 1 | R/W | Whether the descriptor is a valid signal. |

Description: Store the address of the next DMA descriptor. **dma_order_en** is the enable bit of the next DMA descriptor. If this bit is **1**, the next descriptor is valid; if this bit is **0**, the next descriptor is invalid and no operation is performed. When the DMA descriptor is configured, this register holds the address of the next descriptor. After the DMA operation is performed, the **dma_order_en** signal is used to determine whether to start the next DMA operation. In 64-bit address mode, this register stores the low 32-bit address.

DMA_SADDR

Offset address: 0x4

Reset value: 0x00000000

Table 266. DMA_SADDR

| Bit Field | Name | Length | Read/Write | Description |
|-----------|-----------|--------|------------|---|
| 31:0 | dma_saddr | 32 | R/W | System memory address for DMA operations (low 32 bits). |

Description: DMA operations are divided into Memory Read and Memory Write. Memory Read: reads data from memory, saves it in the DMA controller's cache, and then writes it to the AC97 device; this register specifies the address of the read memory. Memory Write: Read data from AC97 device is saved in the DMA cache, and when the data in the DMA cache exceeds a certain number, it is written to the memory, and this register specifies the address of the write memory. In 64-bit address mode, this register stores the low 32-bit address.

DMA_DADDR

Offset address: 0x8

Reset value: 0x00000000

Table 267. DMA_DADDR

| Bit Field | Name | Length | Read/Write | Description |
|-----------|--------------|--------|------------|---|
| 31 | AC97_wr_en | 1 | R/W | AC97 write enable. 1: Indicate a write operation. |
| 30 | AC97_mode | 1 | R/W | 0: mono 1: 2 stereo |
| 29:28 | AC97_wr_mode | 2 | R/W | AC97 write mode. 0: 1-byte 1: 2-byte 2: 4-byte |
| 27:0 | dma_daddr | 28 | R/W | AC97 device address for DMA operation. |

DMA_LENGTH

Offset address: 0xc

Reset value: 0x00000000

Table 268. DMA_LENGTH

| Bit Field | Name | Length | Read/Write | Description |
|-----------|------------|--------|------------|---------------------------------|
| 31:0 | dma_length | 32 | R/W | Transport data length register. |

Description: Represents the length of a piece of content to be carried, in words. When the length of the

word has been carried, the next step is started, i.e. the next loop. When a new loop is started, the length of data is carried again. When step becomes **1**, the single DMA descriptor operation ends and the next descriptor is read.

DMA_STEP_LENGTH

Offset address: **0x10**

Reset value: **0x00000000**

Table 269. DMA_STEP_LENGTH

| Bit Field | Name | Length | Read/Write | Description |
|-------------|-----------------|-----------|------------|--|
| 31:0 | dma_step_length | 32 | R/W | Data transport interval length register. |

Description: The length of the interval between two blocks of memory data being carried, the interval between the end address of the previous step and the start address of the next step.

DMA_STEP_TIMES

Offset address: **0x14**

Reset value: **0x00000000**

Table 270. DMA_STEP_TIMES

| Bit Field | Name | Length | Read/Write | Description |
|-------------|----------------|-----------|------------|--------------------------------------|
| 31:0 | dma_step_times | 32 | R/W | Data transport cycle count register. |

Description: The number of cycles indicates the number of blocks to be carried in a single DMA operation. If you want to carry only one consecutive block, the value of the cycle count register can be assigned to **1**.

DMA_CMD

Offset address: **0x18**

Reset value: **0x00000000**

Table 271. DMA_CMD

| Bit Field | Name | Length | Read/Write | Description |
|--------------|-----------------------|----------|------------|---|
| 14:13 | Dma_cmd | 2 | R/W | Source and destination address generation method. |
| 12 | dma_r_w | 1 | R/W | DMA operation type, 1 is read ddr2 write device, 0 is read device write ddr2. |
| 11:8 | dma_write_state | 4 | R/W | DMA write data status. |
| 7:4 | dma_read_state | 4 | R/W | DMA read data status. |
| 3 | dma_trans_over | 1 | R/W | The DMA has executed all the configured descriptor operations. |
| 2 | dma_single_trans_over | 1 | R/W | The DMA has executed a descriptor operation. |

| Bit Field | Name | Length | Read/Write | Description |
|-----------|--------------|--------|------------|------------------------------------|
| 1 | dma_int | 1 | R/W | DMA interrupt signal. |
| 0 | dma_int_mask | 1 | R/W | Whether DMA interrupts are masked. |

Description: **dma_single_trans_over=1** means the end of one DMA operation, when **length=0** and **step_times=1**, the descriptor of the next DMA operation will be taken. The descriptor address of the next DMA operation is stored in the **DMA_ORDER_ADDR** register. If **dma_order_en=0** in the **DMA_ORDER_ADDR** register, then **dma_trans_over=1** and the whole dma operation is finished and there are no new descriptors to read. If **dma_order_en=1**, then **dma_trans_over** is set to **0** and the next dma descriptor is read. **dma_int** is the interrupt of the DMA, which occurs after a configured DMA operation if there is no interrupt mask. The CPU can set it low directly after processing the interrupt, or it can wait until the DMA makes its next transfer. **dma_int_mask** is the interrupt mask for the corresponding **dma_int**. **dma_read_state** describes the current read state of the DMA. **dma_write_state** describes the current write state of the DMA.

The DMA write state (**WRITE_STATE[3:0]**) describes that the DMA includes the following write states.

Table 272. DMA write state

| Write_state | [3:0] | Description |
|----------------|-------|---|
| Write_idle | 4'h0 | Write state is in idle state |
| W_ddr_wait | 4'h1 | Dma determines that it needs to perform a read device write memory operation and initiates a write memory request, but the memory is not ready to respond to the request, so dma keeps waiting for a response from the memory |
| Write_ddr | 4'h2 | Memory has received a dma write request, but has not yet finished executing the write operation |
| Write_ddr_end | 4'h3 | The memory receives the dma write request and completes the write operation, at which point the dma is in the write memory operation complete state |
| Write_dma_wait | 4'h4 | Dma sends a request to write the dma status register back to memory and waits for memory to receive the request |
| Write_dma | 4'h5 | Memory receives a write dma status request, but the operation is not yet complete |
| Write_dma_end | 4'h6 | Memory completes write dma status operation |
| Write_step_end | 4'h7 | Dma completes a length length operation (i.e. completes a step) |

The DMA read state (**READ_STATE[3:0]**) describes that the DMA includes the following read states.

Table 273. DMA read state

| Read_state | [3:0] | Description |
|------------|-------|---|
| Read_idle | 4'h0 | Read state is in idle state |
| Read_ready | 4'h1 | After receiving the start signal to start the dma operation, enter the ready state and start reading the descriptor |
| Get_order | 4'h2 | Issue a read descriptor request to memory and wait for a memory answer |
| Read_order | 4'h3 | Memory receives a read descriptor request and is performing a read operation |

| Read_state | [3:0] | Description |
|------------------|-------|---|
| Finish_order_end | 4'h4 | Memory read out dma descriptor |
| R_ddr_wait | 4'h5 | Dma sends a read data request to memory and waits for a memory answer |
| Read_ddr | 4'h6 | Memory receives dma read data request and is performing read data operation |
| Read_ddr_end | 4'h7 | Memory completes a read data request from dma |
| Read_dev | 4'h8 | Dma enters read device status |
| Read_dev_end | 4'h9 | The device returns read data, ending the read device request |
| Read_step_end | 4'ha | End a step operation, step times minus 1 |

DMA_ORDER_ADDR_HIGH

Offset address: 0x20

Reset value: 0x00000000

Table 274. DMA_ORDER_ADDR_HIGH

| Bit Field | Name | Length | Read/Write | Description |
|-----------|----------------|--------|------------|---|
| 31:0 | dma_order_addr | 32 | R/W | Memory internal next descriptor address register (high 32 bits) |

DMA_SADDR_HIGH

Offset address: 0x24

Reset value: 0x00000000

Table 275. DMA_SADDR_HIGH

| Bit Field | Name | Length | Read/Write | Description |
|-----------|-----------|--------|------------|---|
| 31:0 | dma_saddr | 32 | R/W | Memory address for DMA operation (high 32 bits) |

Chapter 21. SATA Controller (D8:F0/1/2)

The features of SATA are as follows.

- Supports SATA Generation 1 at 1.5Gbps and SATA Generation 2 at 3Gbps
- Compatible with Serial ATA 2.6 specification and AHCI 1.1 specification

21.1. SATA Configuration Register (D8:F0/1/2)

Table 276. SATA controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|-------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A08h | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 01h | RO |
| 0Ah | SCC | Sub Class Code | 06h | RO |
| 0Bh | BCC | Base Class Code | 01h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 80h | RO |
| 10h-17h | CNL_BAR | Control Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note: Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (SATA - D8:F0/1/2)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 277. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 15:2 | Reserved | RO | Reserved. |
| 1 | Memory Space Enable | R/W | This bit is used to control whether access to the SATA control registers is enabled. 0: Disable access. 1: Enable access to the SATA control registers. The BAR register must be configured before this bit can be configured to 1. |
| 0 | Reserved | RO | Reserved. |

CNL_BAR - Control Base Address Register

This register is used to configure the base address of the control registers of the SATA controller.

Address Offset: 10-13h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 278. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|--|
| 31:13 | Base Address | RW | The software writes to this register field the low address of the base address allocated to the SATA control register. |
| 12:4 | Memory Size | RO | The address space size of SATA control register is 8KB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 14-17h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 279. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:0 | Base Address | RW | The software writes to this register field the high 32-bit address of the base address allocated to the SATA control register. |

21.2. Description of SATA Control Register

The base address of SATA is given by **BAR0** of SATA and the register definition is identical to the protocol standard definition.

Table 280. List of SATA control registers

| Address Offset | Length | Name | Description |
|----------------|--------|-----------|---|
| 0x000 | 32 | CAP | HBA characteristic register |
| 0x004 | 32 | GHC | Global HBA control register |
| 0x008 | 32 | IS | Interrupt status register |
| 0x00c | 32 | PI | Port register |
| 0x010 | 32 | VS | AHCI version register |
| 0x014 | 32 | CCC_CTL | Command completion merge control register |
| 0x018 | 32 | CCC_PORTS | Command completion merge port register |
| 0x024 | 32 | CAP2 | HBA characteristic expansion register |
| 0x0A0 | 32 | BISTAFR | BIST active FIS |
| 0x0A4 | 32 | BISTCR | BIST control register |
| 0x0A8 | 32 | BISTCTR | BIST FIS count register |
| 0x0AC | 32 | BISTSR | BIST status register |
| 0x0B0 | 32 | BISTDECR | BIST double word error count register |
| 0x0BC | 32 | OOBR | OOB register |
| 0x0E0 | 32 | TIMER1MS | 1ms count register |
| 0x0E8 | 32 | GPARAM1R | Global parameter register 1 |
| 0x0EC | 32 | GPARAM2R | Global parameter register 2 |
| 0x0F0 | 32 | PPARAMR | Port parameter register |
| 0x0F4 | 32 | TESTR | Test register |
| 0x0F8 | 32 | VERSIONR | Version register |
| 0x0FC | 32 | IDR | ID register |
| 0x100 | 32 | P0_CLB | Command list base address low 32 bits |
| 0x104 | 32 | P0_CLBU | Command list base address high 32 bits |
| 0x108 | 32 | P0_FB | FIS base address low 32 bits |
| 0x10c | 32 | P0_FBU | FIS base address high 32 bits |
| 0x110 | 32 | P0_IS | Interrupt status register |
| 0x114 | 32 | P0_IE | Interrupt enable register |
| 0x118 | 32 | P0_CMD | Command register |

| Address Offset | Length | Name | Description |
|----------------|--------|-----------|--|
| 0x120 | 32 | P0_TFD | Task file data register |
| 0x124 | 32 | P0_SIG | Signature register |
| 0x128 | 32 | P0_SSTS | SATA status register |
| 0x12C | 32 | P0_SCTL | SATA control register |
| 0x130 | 32 | P0_SERR | SATA error register |
| 0x134 | 32 | P0_SACT | SATA active register |
| 0x138 | 32 | P0_CI | Command send register |
| 0x13C | 32 | P0_SNTF | SATA command notification register |
| 0x170 | 32 | P0_DMACR | DMA control register |
| 0x178 | 32 | P0_PHYCR | PHY control register |
| 0x17C | 32 | P0_PHYSR | PHY status register |
| 0x180 | 32 | P1_CLB | Command list base address low 32 bits |
| 0x184 | 32 | P1_CLBU | Command list base address high 32 bits |
| 0x188 | 32 | P1_FB | FIS base address low 32 bits |
| 0x18c | 32 | P1_FBU | FIS base address high 32 bits |
| 0x190 | 32 | P1_IS | Interrupt status register |
| 0x194 | 32 | P1_IE | Interrupt enable register |
| 0x108 | 32 | P1_CMD | Command register |
| 0x1a0 | 32 | P1_TFD | Task file data register |
| 0x1a4 | 32 | P1_SIG | Signature register |
| 0x1a8 | 32 | P1_SSTS | SATA status register |
| 0x1aC | 32 | P1_SCTL | SATA control register |
| 0x1b0 | 32 | P1_SERR | SATA error register |
| 0x1b4 | 32 | P1_SACT | SATA active register |
| 0x1b8 | 32 | P1_CI | Command send register |
| 0x1bC | 32 | P1_SNTF | SATA command notification register |
| 0x1f0 | 32 | P1_DMACR | DMA control register |
| 0x1f8 | 32 | P1_PHYCR | PHY control register |
| 0x1fC | 32 | P1s_PHYSR | PHY status register |

Chapter 22. PCIE Controller (D9:F0, D10:F0, D11:F0, D12:F0, D13:F0, D14:F0, D15:F0, D16:F0, D17:F0, D18:F0, D19:F0, D20:F0)

The PCIEs of the bridge chip are divided into 5 groups: **PCIE_F0**, **PCIE_F1**, **PCIE_H**, **PCIE_G0**, **PCIE_G1**, with a total of 32 lanes. Each group of PCIE interfaces has its own corresponding control port. The bridge contains 12 PCIE control ports (ports), namely port 0, port 1, port 2, port 3 of **PCIE_F0**, port 0, port 1 of **PCIE_F1**, port 0, port 1 of **PCIE_G0**, port 0, port 1 of **PCIE_G1**, port 0, port 1 of **PCIE_H**, port 1 of **PCIE_H**. Each port corresponds to a PCIE controller, and each PCIE controller contains a TYPE1 type PCI configuration header.

PCIE_F0 includes 4 lanes and can be used as one x4 PCIE or 4 x1 PCIEs. Among them, port 0 controls lane0 in non x4 mode, port 0 controls lane0, and lane0-3 in x4 mode. In non-x4 mode, port 1 controls lane1, port 1 controls lane1, port 2 controls lane2, and port 3 controls lane3.

PCIE_F1 includes 4 lanes, which can be used as one x4 PCIE or 2 x1 PCIEs. Among them, port 0 controls lane0 in non lane0 in non-x4 mode and lane0-3 in x4 mode. In non-x4 mode, port 1 controls lane1, lane2 and lane3 are not available.

PCIE_H includes 8 lanes and can be used as one x8 PCIE or 2 x4 PCIEs. Among them, port 0 controls lane0-3 in non port 0 controls lane0-3 in non-x8 mode and lane0-7 in x8 mode. In non-x8 mode, port 1 controls lane4-7.

PCIE_G0 includes 8 lanes, which can be used as one x8 PCIE or two x4 PCIEs. Among them, port 0 controls lane4-7 in Port 0 controls lane0-3 in non-x8 mode and lane0-7 in x8 mode. In non-x8 mode, port 1 controls lane4-7.

PCIE_G1 includes 8 lanes, which can be used as one x8 PCIE or two x4 PCIEs. Among them, port 0 controls lane4-7 in port 0 controls lane0-3 in non-x8 mode and lane0-7 in x8 mode. In non-x8 mode, port 1 controls lane4-7.

The PCIE controller of the bridge chip can be used only as RC, not as EP.

The configuration methods supported by PCIE and the corresponding control ports are shown in the tables below.

Table 281. Configuration methods and control ports supported by **PCIE_F0**

| lane0 | lane1 | lane2 | lane3 |
|---------|---------|---------|---------|
| x4 (P0) | | | |
| x1 (P0) | x1 (P1) | x1 (P2) | x1 (P3) |

Table 282. Configuration methods and control ports supported by **PCIE_F1**

| lane0 | lane1 | lane2 | lane3 |
|---------|---------|-------|-------|
| x4 (P0) | | | |
| x1 (P0) | x1 (P1) | | |

Table 283. Configuration methods and control ports supported by **PCIE_G0**, **PCIE_G1** and **PCIE_H**

| lane0 | lane1 | lane2 | lane3 | lane4 | lane5 | lane6 | lane7 |
|---------|-------|-------|-------|-------|-------|-------|-------|
| x8 (P0) | | | | | | | |

| | |
|---------|---------|
| x4 (P0) | x4 (P1) |
|---------|---------|

22.1. PCI Configuration Register

The following table lists the configuration header defaults for PCIE ports, the Device ID may be different for different ports, all other fields are the same.

Table 284. PCIE controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|---|------------------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | See description of registers | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 06h-07h | PCISTS | PCI Status | 0010h | RO |
| 08h | RID | Revision ID | 01h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 04h | RO |
| 0Bh | BCC | Base Class Code | 06h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Dh | PLT | Primary Latency Timer | 00h | RO |
| 0Eh | HEADTYP | Header Type | 01h | RO |
| 10h-17h | CNL_BAR | Control Block Base Address Register | 0000000000000004h | R/W, RO |
| 18h | PBNUM | Primary Bus Number | 00h | R/W |
| 19h | SBNUM | Secondary Bus Number | 00h | R/W |
| 1Ah | SUBNUM | Subordinate Bus Number | 00h | R/W |
| 1Bh | SLT | Secondary Latency Timer | 00h | RO |
| 1Ch | IOBASE | I/O Base | 01h | R/W |
| 1Dh | IOLMT | I/O Limit | 01h | R/W |
| 1Eh-1Fh | SSTS | Secondary Status | 0000h | RO |
| 20h-21h | MBASE | Memory Base | 0000h | R/W |
| 22h-23h | MLMT | Memory Limit | 0000h | R/W |
| 25h-24h | PMBASE | Prefetchable Memory Base | 0000h | R/W |
| 27h-26h | PMLMT | Prefetchable Memory Limit | 0000h | R/W |
| 28h-2Bh | PMBU32 | Prefetchable Memory Base Upper 32 Bits | 00000000h | R/W |
| 2Ch-2Fh | PMLU32 | Prefetchable Memory Limit Upper 32 Bits | 00000000h | R/W |
| 30h-31h | IOBU | I/O Base Upper 16 Bits | 0000h | R/W |
| 32h-33h | IOLMTU | I/O Limit Upper 16 Bits | 0000h | R/W |

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|-------------------------|---------------|------------|
| 34h | CAPP | Capabilities Pointer | 40h | RO |
| 3Ch | INT_LN | Interrupt Line | FFh | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |
| 3Eh-3Fh | BCTRL | Bridge Control Register | 0000h | R/W |

Note: Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

DID - Device Identity Register (PCIE)

Address Offset: 02-03h

Attribute: RO

Default value: See description

Size: 16 bits

Table 285. Device identity register

| Bit Field | Name | Read/Write | Description |
|-----------|------|------------|---|
| 15:0 | DID | RO | PCIE device identity register. The corresponding DID of each PCIE port is shown in the following table. |

Table 286. Table of DID of PCIE port

| PCI Device Number | Description | Device Identity Register |
|-------------------|----------------|--------------------------|
| D9:F0 | PCIE_F0 port 0 | 7A19h |
| D10:F0 | PCIE_F0 port 1 | 7A09h |
| D11:F0 | PCIE_F0 port 2 | 7A09h |
| D12:F0 | PCIE_F0 port 3 | 7A09h |
| D13:F0 | PCIE_F1 port 0 | 7A19h |
| D14:F0 | PCIE_F1 port 1 | 7A09h |
| D15:F0 | PCIE_G0 port 0 | 7A29h |
| D16:F0 | PCIE_G0 port 1 | 7A19h |
| D17:F0 | PCIE_G1 port 0 | 7A29h |
| D18:F0 | PCIE_G1 port 1 | 7A19h |
| D19:F0 | PCIE_H port 0 | 7A29h |
| D20:F0 | PCIE_H port 1 | 7A19h |

Note:

1. The correct value of the subclass code for all PCIe controllers integrated in the bridge should be 0x04 for the PCI-to-PCI bridge, but this bridge incorrectly implements this value as 0x00 (for the Host bridge). The software needs to ignore this bit field and still handle the bridge-integrated PCIe controllers as PCI-to-PCI bridges, see [Notes on the Use of the Software](#).
2. Only one device (Device 0) can be mounted on the bus below all PCIe controllers integrated in the bridge, but when the software scans the PCIe bus for non-Device 0 devices, this PCIe controller will return the information of Device 0, causing Device 0 to be discovered repeatedly. Therefore, the software must not actively scan for non-Device 0 devices below the PCIe controller, see [Notes on the Use of the Software](#).

22.2. Address Space Division

The PCIe controller in the bridge has a standard PCIe configuration header, so the internal registers of the PCIe controller and the address space of its downstream devices are managed by the information in its configuration header. The address-related registers in the configuration header are determined during the PCI device scan.

Because the bridge's PCIe controller can only operate in RC mode, its configuration header is of type TYPE1.

Each PCIe port acts as a separate device in the bridge slice, and each port contains a PCIe configuration header. When the PCIe is operating in X4 mode, the port software for the other X1 is not visible, and the other X1 ports are only accessible when the PCIe is operating in X1 mode.

For each PCIe port, the address space can be divided into the following parts.

Configuration header address space: This part of the space corresponds to the configuration header of the PCIe and is accessed through configuration requests up to 4KB. See [Access Address of the PCI Configuration](#) for accessing address space above 256B.

Configuration Access Address Space: This portion of the address space is used to access the PCIe controller's downstream device configuration header information via configuration requests. Depending on the Bus number of the downstream device, it is up to the PCIe controller to decide whether to send a TYPE0 type or TYPE1 type configuration access.

The addresses of the above two address spaces are calculated from the configuration address space base address, BUS number, device number, function number, and register offset address, and can be accessed by word.

PCIe controller internal register space: This part of the address space is used to access the internal registers of the PCIe controller. These registers are used to control the behavior and characteristics of the PCIe controller and belong to two address spaces with the PCIe configuration header space. This address space is of type MEM, 64-bit address space, 4KB in size, with a base address equal to the value of 64-bit BAR0, which is assigned by the PCI scan software during initialization.

MEM address space: This part of the address space contains all the MEM address space of the devices downstream of the PCIe controller. For the 32-bit address space, this is determined by the memory base and memory limit of the PCIe configuration header. For the 64-bit address space, this is determined by the prefetchable memory base (combined upper 32 bits) and prefetchable memory limit (combined upper 32 bits) of the PCIe configuration header. This address space is enabled and controlled by the command register bit1 of the PCIe configuration header.

I/O address space: This part of the address space contains all the I/O address space of the devices downstream of the PCIe controller. It is determined by the IO base (combined upper 16 bits) and IO limit (combined upper 16 bits) of the PCIe configuration header. This address space is enabled and controlled by the command register bit0 of the PCIe configuration header.

For the MEM address space and I/O address space, if there is no device connected downstream of an X1

port in X1 operation mode, the MEM and I/O address space can be disabled by setting **bit0** and **bit1** of the command register to **0**.

PCIE Controller Enable

General configuration register 0 of the bridge configuration register contains the enable bits for the PCIE controller. It needs to be enabled when using the corresponding PCIE controller in order to access all address spaces of that controller and downstream devices, including configuration access to the controller.

22.3. Special Notes

PCIE Capability

The maximum MPS (Max Payload Size) and MRRS (Max Read Request Size) supported by the integrated PCIE controller of the bridge are both 256 bytes. The MPS setting can be set under the BIOS through the PCI negotiation mechanism. Since there is no negotiation mechanism for MRRS, BIOS developers need to set the MRRS value of the device to a value no larger than 256 bytes.

PCIE MSI

On 3A+7A systems, the destination address for PCI MSI interrupts is **0xfdf8000000** or **0x2ff00000**. The bridge converts the MSI message packets sent by the device to these two address segments into HT interrupt message packets and sends them to the processor.

PCIE Controller Performance

The PCIE controllers integrated in the bridge are x8, x4, and x1. The P0 control port of **PCIE_G0/G1/H** is the x8 controller, the P0 port of **PCIE_F0/F1** and the P1 port of **PCIE_G0/G1/H** are the x4 controllers, and the P1/P2/P3 port of **PCIE_F0** and the P1 port of **PCIE_F1** are the x1 controllers.

These three controllers have different numbers of internal flow-controlled buffers, with x8, x4, and x1 controllers decreasing in order, so for some high-bandwidth PCIE devices, using a controller with a larger number of flow-controlled buffers for the same data width will result in a performance improvement. Therefore, it is recommended to give preference to controllers with larger number of flow control buffers.

Chapter 23. SPI Controller (D22:F0)

23.1. SPI Configuration Register (D22:F0)

Table 287. SPI controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|-------------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A0Bh | RO |
| 04h-05h | PCICMD | PCI Command | 0000h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 08h | RO |
| 0Bh | BCC | Base Class Code | 80h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 00h | RO |
| 10h-17h | CBAR | Control Base Address Register | 0000000000000004h | R/W, RO |
| 18h-1Fh | MBAR | Memory Base Address Register | 0000000000000004h | R/W, RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note: Address space not listed in the table indicates reserved.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (SPI - D22:F0)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 288. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 15:2 | Reserved | RO | Reserved. |

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 1 | Memory Space Enable | R/W | This bit is used to control whether access to the SPI control registers and SPI memory space is enabled. 0: Disable access. 1: Enable access to the SPI control registers and SPI memory space. The BAR register must be configured before this bit can be configured to 1. |
| 0 | Reserved | RO | Reserved. |

The SPI controller consists of two address spaces: the control register space and the memory space.

CNL_BAR - Control Base Address Register

This register is used to configure the base address of the control registers of the SPI controller.

Address Offset: 10-13h

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 289. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 31:12 | Base Address | RW | The software writes to this register field the low address of the base address allocated to the SPI controller. |
| 11:4 | Memory Size | RO | The address space size of SPI controller is 4KB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 14-17h

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 290. Control base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|---|
| 31:0 | Base Address | RW | The software writes to this register field the high 32-bit address of the base address allocated to the SPI controller. |

MBAR - MEM Space Base Address Register

This register is used to configure the MEM space base address of the SPI controller.

Address Offset: 18-1Bh

Attribute: R/W, RO

Default value: 00000004h

Size: 32 bits

Table 291. MEM space base address register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 31:24 | Base Address | RW | The software writes to this register field the bit[31:24] of the base address allocated to the SPI MEM space. |
| 23:4 | Memory Size | RO | The SPI MEM space size is 16MB. |
| 3 | Prefetchable Memory | RO | Set to 0 to indicate that it is not prefetchable. |
| 2:1 | Memory Type | RO | Set to 10b to indicate 64-bit BAR. |
| 0 | Memory/ I/O Space | RO | Set to 0 to indicate Memory space BAR. |

Address Offset: 1C-1Fh

Attribute: R/W

Default value: 00000000h

Size: 32 bits

Table 292. MEM space base address register

| Bit Field | Name | Read/Write | Description |
|-----------|--------------|------------|--|
| 31:0 | Base Address | RW | The software writes to this register field the high 32-bit address of the base address allocated to the SPI MEM space. |

23.2. SPI Control Register

Table 293. List of SPI control registers

| Address Offset | Name | Description |
|----------------|------|------------------|
| 0 | SPCR | Control register |
| 1 | SPSR | Status register |

| Address Offset | Name | Description |
|----------------|---------------|------------------------------|
| 2 | TxFIFO/RxFIFO | Data register |
| 3 | SPER | External register |
| 4 | SFC_PARAM | Parameter control register |
| 5 | SFC_SOFTCS | Chip select control register |
| 6 | SFC_TIMING | Timing control register |

Control Register (SPCR)

Offset address: 0x0

Table 294. Control register

| Bit Field | Name | Read/Write | Initial Value | Description |
|-----------|----------|------------|---------------|---|
| 7 | spie | R/W | 0 | Interrupt output enable signal (active high) |
| 6 | spe | R/W | 0 | System operation enable signal (active high) |
| 5 | Reserved | RO | 0 | Reserved |
| 4 | mstr | RO | 1 | master mode select bit. This bit is always held 1 |
| 3 | cpol | R/W | 0 | Clock polarity bits |
| 2 | cpha | R/W | 0 | Clock phase. 1 is opposite phase, and 0 is same |
| 1:0 | spr | R/W | 0 | sclk_o frequency division configuration. It need to be used with sper's `spre |

Status Register (SPSR)

Offset address: 0x1

Table 295. Status register

| Bit Field | Name | Read/Write | Initial Value | Description |
|-----------|----------|------------|---------------|--|
| 7 | spif | R/W | 0 | Interrupt flag. 1 indicates an interrupt request, write 1 to clear |
| 6 | wcol | R/W | 0 | Write register overflow flag bit. 1 indicates overflowed, write 1 to clear |
| 5:4 | Reserved | RO | 0 | Reserved |
| 3 | wffull | RO | 0 | Write register full. 1 indicates full |
| 2 | wfempty | RO | 1 | Write register empty. 1 indicates empty |
| 1 | rffull | RO | 0 | Read register full. 1 indicates full |
| 0 | rfempty | RO | 1 | Read register empty. 1 indicates empty |

Data Register (TxFIFO/RxFIFO)

Offset address: 0x2

Table 296. Data register

| Bit Field | Name | Read/Write | Initial Value | Description |
|-----------|---------------|------------|---------------|--|
| 7:0 | TxFIFO RxFIFO | W RO | - | Data transporting port. Data receiving port |

External Register (SPER)

Offset address: 0x3

Table 297. External register

| Bit Field | Name | Read/Write | Initial Value | Description |
|-----------|------|------------|---------------|---|
| 7:6 | icnt | R/W | 0 | Bytes transferred before sending an interrupt. 00: 1 01: 2 10: 3 11: 4 |
| 5:3 | - | - | - | Reserved |
| 2 | mode | R/W | 0 | SPI interface mode control 0: Sampling and transporting timing are simultaneous 1: Sampling and transporting timing staggered by half a cycle |
| 1:0 | spre | R/W | 0 | Set the ratio of the frequency division together with spr |

Table 298. SPI Frequency Division Factor

| | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|-----|-----|-----|------|------|------|
| spre | 00 | 00 | 00 | 00 | 01 | 01 | 01 | 01 | 10 | 10 | 10 | 10 |
| spr | 00 | 01 | 10 | 11 | 00 | 01 | 10 | 11 | 00 | 01 | 10 | 11 |
| Frequency Division Factor | 2 | 4 | 16 | 32 | 8 | 64 | 128 | 256 | 512 | 1024 | 2048 | 4096 |

Parameter Control Register (SFC_PARAM)

Offset address: 0x4

Table 299. Parameter control register

| Bit Field | Name | Read/Write | Initial Value | Description |
|-----------|-----------|------------|---------------|---|
| 7:4 | clk_div | R/W | 2 | Clock division number selection. The frequency division factor is the same as the combination of {spre, spr} |
| 3 | dual_io | R/W | 0 | Dual I/O mode with higher priority than fast read |
| 2 | fast_read | R/W | 0 | Fast Read Mode |
| 1 | burst_en | R/W | 0 | SPI flash supports sequential address read mode |
| 0 | memory_en | R/W | 1 | SPI flash read enable. When disabled, csn[0] can be controlled by software |

Chip Select Control Register (SFC_SOFTCS)

Offset address: 0x5

Table 300. Chip select control register

| Bit Field | Name | Read/Write | Initial Value | Description |
|-----------|------|------------|---------------|--|
| 7:4 | csn | R/W | 0 | csn pin output value |
| 3:0 | csen | R/W | 0 | When the bit is 1, the csn line of the corresponding bit is controlled by 7:4 bits |

Timing Control Register (SFC_TIMING)

Offset address: 0x6

Table 301. Timing control register

| Bit Field | Name | Read/Write | Initial Value | Description |
|-----------|-------|------------|---------------|---|
| 7:3 | - | - | - | Reserved |
| 2 | tFAST | R/W | 0 | SPI flash read sampling mode 0: Rising edge sampling, half SPI cycle interval 1: Rising edge sampling with one SPI cycle interval |

| Bit Field | Name | Read/Write | Initial Value | Description |
|-----------|------|------------|---------------|--|
| 1:0 | tCSH | R/W | 3 | <p>The minimum invalidation time of the SPI Flash's chip select signal, in terms of the clock period after frequency division.</p> <p>Calculation of T</p> <p>00: 1T</p> <p>01: 2T</p> <p>10: 4T</p> <p>11: 8T</p> |

23.3. SPI Software Programming Guide

Read and Write Operations of the SPI Host Controller

Module Initialization

1. Stop SPI controller operation, write 0 to the spe bit of control register spcr.
2. Reset the status register spsr and write 1100_0000b to the register.
3. Set the external register sper, including the interrupt request condition sper[7:6] and the dividing factor sper[1:0], refer to the register description for details.
4. Configure SPI timing, including cpol, cpha of spcr and mode of sper. mode is 1 for standard SPI implementation and 0 for compatible mode.
5. Configure interrupt enable, spie bit of spcr.
6. Start the SPI controller and write 1 to the spe bit of the control register spcr.

Send/transport Operations of the Module

1. Write data to the data transport register.
2. Since transporting and receiving occur simultaneously, the SPI slave device must perform a readout operation even if no valid data is sent.

Interrupt Handling

1. Receive the interrupt request.
2. Read the value of status register spsr, if spsr[2] is 1, it means data transport is completed, if spsr[0] is 1, it means data has been received.
3. Read or write the data transport register.
4. Write 1 to the spif bit of status register spsr to clear the controller's interrupt request.

Hardware SPI Flash Read

Initialization

1. Write 1 to the memory_en bit of SFC_PARAM.

2. Set the read parameters (clock division, sequential address read, fast read, dual I/O, tCSH, etc.). These parameters are reset to the most conservative values.

Changing Parameters

If the SPI Flash used supports higher frequencies or offers enhanced features, modifying the corresponding parameters can greatly speed up the Flash access speed. The parameter modification does not require turning off the SPI Flash read enable (`memory_en`). Refer to the description of registers for details.

Chapter 24. LPC Controller (D23:F0)

The LPC controller has the following features.

- Compliant with LPC1.1 specification
- Supports LPC access timeout counter
- Supports Memory Read/Write access type
- Supports Firmware Memory Read/Write access type (single byte)
- Support I/O read/write access type
- Support TPM I/O read/write access type
- Support Memory access type address conversion
- Support Serial IRQ specification, support 17 interrupt sources

24.1. LPC Configuration Register (D23:F0)

Table 302. LPC controller configuration registers

| Address Offset | Abbreviation | Description | Default value | Read/Write |
|----------------|--------------|--------------------------|-------------------|------------|
| 00h-01h | VID | Vendor ID | 0014h | RO |
| 02h-03h | DID | Device ID | 7A0Ch | RO |
| 04h-05h | PCICMD | PCI Command | 0001h | R/W, RO |
| 08h | RID | Revision ID | 00h | RO |
| 09h | PI | Programming Interface | 00h | RO |
| 0Ah | SCC | Sub Class Code | 01h | RO |
| 0Bh | BCC | Base Class Code | 06h | RO |
| 0Ch | CLS | Cache Line Size | 00h | RO |
| 0Eh | HEADTYP | Header Type | 00h | RO |
| 10h-17h | FIXCREG* | Fixed Control Register | 0000000010002004h | RO |
| 18h-1Fh | FIXMREG* | Fixed Memory Register | 0000000012000004h | RO |
| 20h-27h | FIXIOREG* | Fixed I/O Register | 000000FDFC000001h | RO |
| 2Ch-2Dh | SVID | Subsystem Vendor ID | 0000h | RO |
| 2Eh-2Fh | SID | Subsystem Identification | 0000h | RO |
| 3Ch | INT_LN | Interrupt Line | 00h | R/W |
| 3Dh | INT_PN | Interrupt Pin | 01h | RO |

Note: Address space not listed in the table indicates reserved.

* See the subsequent FIXCREG/FIXMREG/FIXIOREG and Appendix 2 for more information.

Registers that differ slightly from the PCI configuration header specification and their descriptions are listed below.

PCICMD - PCI Command Register (LPC - D23:F0)

Address Offset: 04-05h

Attribute: R/W, RO

Default value: 0000h

Size: 16 bits

Table 303. PCI command register

| Bit Field | Name | Read/Write | Description |
|-----------|---------------------|------------|---|
| 15:2 | Reserved | RO | Reserved. |
| 1 | Memory Space Enable | R/W | This bit is used to control whether access to the LPC control registers and MEM space is enabled. 0: Disable access. 1: Enable access to the LPC control registers and MEM space |
| 0 | I/O Space Enable | R/W | This bit is used to control whether access to the LPC I/O space is enabled. The address of the LPC I/O space is fixed starting from address 0 of the I/O space. 0: Disable access. 1: Enable access to the LPC I/O space. |

FIXCREG - Fixed Control Register

This register is not used as the BAR of the LPC configuration header.

Address Offset: 10-17h

Attribute: RO

Default value: 0000000010002004h

Size: 64 bits

Table 304. Fixed control register

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 63:0 | Reserved | RO | Reserved. |

FIXMREG - Fixed MEM Register

This register is not used as the BAR of the LPC configuration header.

Address Offset: 18-1Fh

Attribute: RO

Default value: 0000000012000004h

Size: 64 bits

Table 305. Fixed MEM register

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 63 : 0 | Reserved | RO | Reserved. |

FIXIOREG - Fixed I/O Register

This register is not used as the BAR of the LPC configuration header.

Address Offset: 20-27h

Attribute: RO

Default value: 000000FDFC000001h

Size: 64 bits

Table 306. Fixed I/O register

| Bit Field | Name | Read/Write | Description |
|-----------|----------|------------|-------------|
| 63 : 0 | Reserved | RO | Reserved. |

The addresses of **FIXCREG**, **FIXMREG**, and **FIXIOREG** are the same as the **BAR** registers of the PCI configuration header, but these registers are not used as the **BAR** registers of the LPC configuration header. Software can work around this hardware bug by modifying the PCI configuration read function so that the upper layer software is not affected. See [Notes on the Use of the Software](#) for more details.

24.2. LPC Access Address

The LPC controller consists of three address spaces: the control register space, the MEM space, and the I/O space.

The LPC control register space is used to configure the LPC controller, which is located in the fixed device address space of the bridge chip, starting at 0x1000, 2000, with a size of 4KB.

The LPC MEM space is used to access the Memory/Firmware Memory devices mounted on the LPC bus. The LPC MEM space is located in the fixed device address space of the bridge chip starting at 0x1200, 0000 and is 32MB in size. Processor accesses to the LPC MEM space are converted to LPC protocol Memory accesses and sent to the LPC bus. Which type of Memory access is issued by the LPC controller is determined by the LPC controller's control registers. Addresses sent by the processor to this address space can be address converted. The converted address is set by the LPC controller's configuration register (**LPC_MEM_TRANS**).

24.3. LPC Interrupt

The LPC controller internally includes two types of interrupts: SIRQ interrupts and access timeout interrupts. The LPC controller supports a total of 17 SIRQ interrupts, corresponding to the **bits[16:0]** of the interrupt-related register. The access timeout interrupt corresponds to the **bit[17]** of the interrupt-related register.

The SIRQ interrupt is a level-triggered interrupt, and the value of the trigger level can be configured by the

register. The software should configure the trigger level of the SIRQ interrupt before enabling the SIRQ interrupt of the LPC controller. The SIRQ interrupt does not need to be cleared by software.

The access timeout interrupt is edge-triggered, so if an LPC access timeout interrupt occurs, the software needs to write `bit[17]` of the interrupt clear register to clear the interrupt.

24.4. LPC Control Register

Control Register 0

Address Offset: `00-03h`

Attribute: R/W

Default value: `0000FFFFh`

Size: `4`

Table 307. Control register 0

| Bit Field | Name | Read/Write | Description |
|--------------------|-------------------------------|------------|---|
| <code>31</code> | <code>SIRQ_EN</code> | R/W | SIRQ interrupt enable control. |
| <code>23</code> | <code>LPC_MEM_TRANS_EN</code> | R/W | LPC Memory space address translation enable. |
| <code>22:16</code> | <code>LPC_MEM_TRANS</code> | R/W | The high 7-bit address (<code>bit[31:25]</code>) of the LPC Memory space after address translation. |
| <code>15:0</code> | <code>LPC_SYNC_TIMEOUT</code> | R/W | Threshold for LPC access timeout (minimum value 64). |

Control Register 1

Address Offset: `04-07h`

Attribute: R/W

Default value: `00000000h`

Size: `4`

Table 308. Control register 1

| Bit Field | Name | Read/Write | Description |
|-------------------|----------------------------|------------|--|
| <code>31</code> | <code>FIRMWARE_TYPE</code> | R/W | LPC Memory space Firmware Memory access type configuration. |
| <code>17:0</code> | <code>LPC_INT_EN</code> | R/W | LPC interrupt enable, each bit corresponds to an interrupt source. For each interrupt source: <code>0</code> : Disable interrupt. <code>1</code> : Enable interrupt. |

LPC Interrupt Status Register

Address Offset: 08-0Bh

Attribute: R/W

Default value: 00000000h

Size: 4

Table 309. LPC interrupt status register

| Bit Field | Name | Read/Write | Description |
|-----------|-------------|------------|---|
| 17:0 | LPC_INT_SRC | RO | LPC Interrupt source indication, each bit corresponds to an interrupt source. For each interrupt source: 0: Disable interrupt. 1: Enable interrupt. |

LPC Interrupt Clear Register

Address Offset: 0C-0Fh

Attribute: WO

Default value: 00000000h

Size: 4

Table 310. LPC interrupt clear register

| Bit Field | Name | Read/Write | Description |
|-----------|-----------------------|------------|---|
| 17 | LPC_TIMEOUT_INT_CLEAR | WO | LPC access timeout interrupt clear (write 1 to clear). Bit 17 corresponds to LPC access timeout interrupt. Write 1 to clear, write 0 to be invalid. |

LPC SIRQ Interrupt Polarity Register

Address Offset: 10-13h

Attribute: R/W

Default value: 0000FFFBh

Size: 4

Table 311. LPC SIRQ interrupt polarity register

| Bit Field | Name | Read/Write | Description |
|-----------|-------------------|------------|---|
| 16:0 | SIRQ_INT_POLARITY | R/W | <p>LPC SIRQ interrupt polarity register, each bit corresponds to an interrupt source. For each interrupt source:</p> <p>0: Low level trigger.</p> <p>1: High level trigger.</p> |

Appendix A: Table of Pin Multiplexing

The chip pins are multiplexed as shown in the following table.

Table 312. Table of chip pin function multiplexing

| Function 0 (Default) | Function 1 | Function 2 | Function 3 |
|------------------------|------------|-----------------------|------------|
| VSB_GATE _n | GPI001 | | |
| CLKOUT25M | GPI002 | | |
| CLKOUTFLEX | GPI003 | | |
| PWM0 | GPI004 | | |
| PWM1 | GPI005 | | |
| PWM2 | GPI006 | | |
| PWM3 | GPI007 | | |
| I2C0_SCL | GPI008 | | |
| I2C0_SDA | GPI009 | | |
| I2C1_SCL | GPI010 | | |
| I2C1_SDA | GPI011 | | |
| SPI_CS _n 0 | GPI012 | I2C4_SCL | |
| SPI_CS _n 1 | GPI013 | I2C4_SDA | |
| SPI_CS _n 2 | GPI014 | I2C5_SCL | |
| SPI_CS _n 3 | GPI015 | I2C5_SDA | |
| SPI_SDI | GPI016 | | |
| SPI_SD0 | GPI017 | | |
| SPI_SCK | GPI018 | | |
| HDA_BITCLK | GPI019 | AC97_BITCLK | |
| HDA_SYNC | GPI020 | AC97_SYNC | |
| HDA_RESET _n | GPI021 | AC97_RST _n | |
| HDA_SD0 | GPI022 | AC97_SD0 | |
| HDA_SDI0 | GPI023 | AC97_SDI | |
| HDA_SDI1 | GPI024 | | |
| HDA_SDI2 | GPI025 | | |
| SATA0_LED _n | GPI026 | | |
| SATA1_LED _n | GPI027 | | |
| SATA2_LED _n | GPI028 | | |
| USB_OC_0 | GPI029 | | |
| USB_OC_1 | GPI030 | | |
| USB_OC_2 | GPI031 | | |

| | | | |
|------------------------|--------|----------|----------|
| UART3_RXD | GPI032 | UART_DCD | I2C2_SCL |
| UART3_TXD | GPI033 | UART_RI | I2C2_SDA |
| UART2_RXD | GPI034 | UART_DSR | I2C3_SCL |
| UART2_TXD | GPI035 | UART_DTR | I2C3_SDA |
| UART1_RXD | GPI036 | UART_CTS | |
| UART1_TXD | GPI037 | UART_RTS | |
| UART0_RXD | GPI038 | UART_RXD | |
| UART0_TXD | GPI039 | UART_TXD | |
| LPC_AD0 | GPI040 | | |
| LPC_AD1 | GPI041 | | |
| LPC_AD2 | GPI042 | | |
| LPC_AD3 | GPI043 | | |
| LPC_SERIRQ | GPI044 | | |
| LPC_FRAME _n | GPI045 | | |
| SYS_CLKSEL0 | GPI046 | | |
| SYS_CLKSEL1 | GPI047 | | |
| SYS_CLKSEL2 | GPI048 | | |
| SYS_CLKSEL3 | GPI049 | | |
| SYS_CLKSEL4 | GPI050 | | |
| SYS_CLKSEL5 | GPI051 | | |
| SYS_CLKSEL6 | GPI052 | | |
| SYS_CLKSEL7 | GPI053 | | |
| SYS_PCIEBRGMODE | GPI054 | | |
| HT_8x2 | GPI055 | | |
| SYS_CLKSEL8 | GPI056 | | |

Note: All signals of HDA and LPC can only be multiplexed as a whole, and each pin cannot be controlled individually. For example, if the AC97 function is enabled, pin **HDA_SDI1/2** cannot be used as other functions.

Appendix B: Notes on the Use of the Software

Currently, there are five^[1] problems that need to be fixed by the software for the bridge piece.

1. PCI device scanning problem

The correct value of the subclass code of the PCI device header of the PCIE bridge integrated in the bridge chip should be `0x04` (for PCI type bridge), but this bridge chip will now be `0x00` (for Host type bridge).

Solution: When the read configuration header access is found, if the access address is bus 0 of the device 9 to 20 and the address is `0x8`, directly return `0x06040001`, and not return the hardware read value.

2. PCI device scanning problem

For the PCIE bridge integrated in the bridge chip, when scanning the lower bus, when scanning the non-0 device, it should return an invalid value, but this bridge chip will return the configuration header of the 0 device, causing the 0 device to be found repeatedly.

Solution: For PCIE bridges integrated in the bridge, the lower bus only scans for device 0 and no other device number is scanned.

3. PCI device scanning problem

The **Memory Space Enable** control bits of the PCI configuration headers of the OHCI (Function 0) and EHCI (Function 1) controllers of the USB devices (Device 4 and Device 5) are reversed. That is, the **Memory Space Enable** bit of EHCI controls the Mem space enable of OHCI, while the **Memory Space Enable** bit of OHCI controls the Mem space enable of EHCI.

Solution: Fix by software.

4. GMAC DMA64 problem

In 64-bit DMA mode, the high 32-bit register (`0x1094`) of the GMAC's transmit descriptor base address can only be read, but not written.

Solution: Write to the high 32-bit register (`0x1094`) by writing the following addresses `{0x10a8[31:8], 0x1068[7:0]}`.

5. LPC **FIXIOREG** problem

The **FIXCREG**/**FIXMREG**/**FIXIOREG** of the LPC is used as an internal reserved register and is not used as a BAR in the PCI configuration header, but the hardware implementation incorrectly places its address in the location of the PCI configuration header BAR. The software should treat the **BAR** register location of the LPC as an invalid BAR, but needs to enable I/O and MEM space access for the LPC.

Solution: In the PCI configuration read access function, when the device found to be read is LPC (`B0:D23:F0`) and the address is equal to the address of **BAR0/1/2/3/4/5** (`0x10` to `0x27`), return data `0` directly.

6. Concurrent access of DC control registers problem

The DC's control registers do not support simultaneous write accesses by multiple processors, regardless of whether the destination registers for these write accesses are the same. That is, only one processor can write to the DC's control register space at any given time.

Solution: The kernel prevents multiple processors from writing to the DC control register space at the same time by adding a lock.

1. Translator's note: Maybe six.